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A low-noise small signal sensing scheme in voltage mode for high density magnetoresistive memories

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A low noise small signal sensing scheme in voltage mode for high density magnetoresistive memories

by

K. T. Manel Ranmuthu

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Members of the Committee:

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Iowa State University
Ames, Iowa

1993

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1. INTRODUCTION

1.1 A Historical Note

Memory ICs designed for space and military applications are expected to meet a set of stringent requirements in order to maintain reliability in a hostile environment. Nonvolatility, low power consumption, radiation hardness and a wide temperature operating range are some of those. For a long time, only plated wire memories were able to meet the above criteria.

Magnetoresistive random access memories (MRAMs) were originally developed as a replacement technology for plated wire memories which consume high power, have large cells that do not scale and are expensive. The basic memory cell of this technology, which successfully combines integrated circuit and magnetic thin film processes to fabricate nonvolatile and random access memory ICs, was developed and patented by Dr A V Pohm and Dr J M Daughton in 1983.

1.2 The Memory Cell and Access Mechanism

The MR memory technology is based on two fundamental material properties of thin magnetic films [2]. One is the preference for the magnetization to lie along a single axis in one of two anti-parallel states, which is known as uniaxial anisotropy (Figure 1.1). This

preferred axis--called the easy axis--is determined by the direction of a strong magnetic orienting field applied during film deposition and/or annealing.

The other fundamental property is magnetoresistance, or the change in the electrical resistance caused by an applied magnetic field. This change in resistance depends on the angle the current makes with the magnetization according to the formula,

$$R = R_0 + \Delta R \cos^2 \Theta \qquad (1.1)$$

where

R_0 = the resistance when the current and magnetization are perpendicular to each other

ΔR = magnetoresistance term

Θ = angle between the current and the magnetization

The ratio $\Delta R/R$ is called the MR coefficient (C_{MR}) and it is ordinarily between 0.01 and 0.06 for most ferromagnetic alloys.

Storage of a bit in a MRAM cell uses the anisotropic nature of the film. Whether it is a "1" or a "0" depends on which anti-parallel state along the easy axis the magnetization vector is in (Figure 1.1). The sensing of a stored bit makes use of magnetoresistance, i.e., the change of resistance with current in the presence of a magnetic field.

The basic storage cell is a sandwich structure made of two 150 °A layers of magnetic film (65% Ni, 15% Fe and 20% Co) separated by a 50 °A non-magnetic layer (Ta). The design is such that the uniaxial anisotropy axis of the magnetic film is perpendicular to the long dimension of the element (Figure 1.2). Thus, in remnant "1" or "0" states, the magnetization points across the cell with the magnetizations in the two films oppositely directed (Figure 1.3). This greatly reduces the demagnetizing fields and permits high cell density.

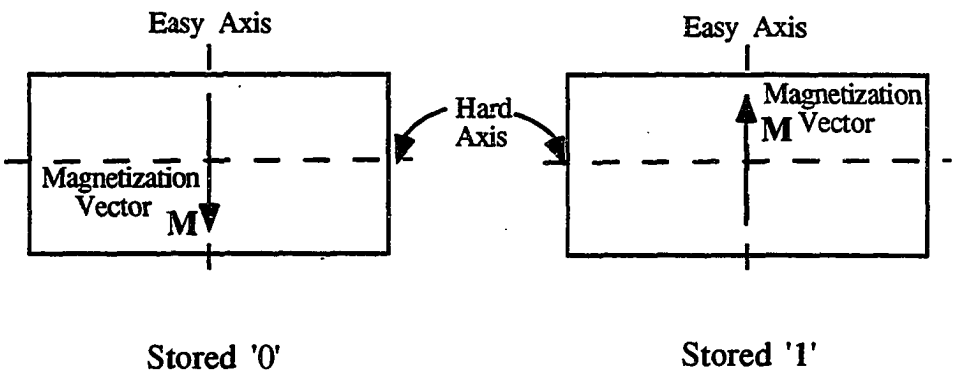


Figure 1.1 : Use of Uniaxial Anisotropy for Data Storage

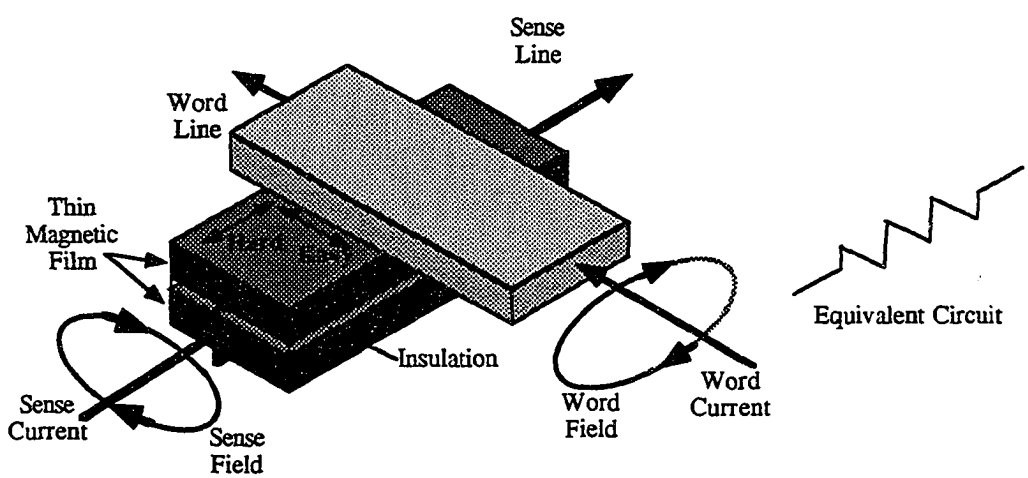
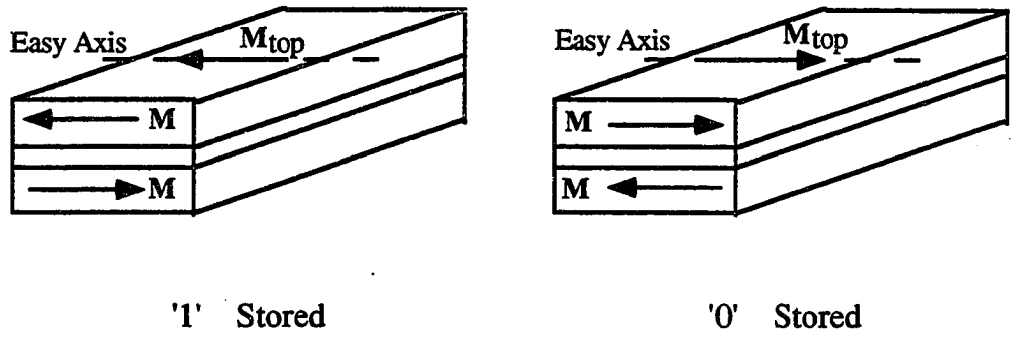


Figure 1.2: Basic MRAM Cell



'1' Stored '0' Stored

Figure 1.3 : Orientation of Magnetization in a Memory Cell

A memory cell is accessed by applying a "sense" current (I_S) through the cell itself together with a "word" current (I_W) through the overlaid, orthogonal word line which is electrically isolated from the cell (Figure 1.2). The resultant magnetic field generated by these two currents produces the required switching or rotation of the magnetization vector (**M**).

When writing a bit, Is provides the easy-direction magnetic field. (Positive I_S stores a "0".) The magnetization vector (**M**) switches only if the sense field (H_S) applied by the sense current (I_S) opposes **M**, and the resultant applied magnetic amplitude $|H_S + H_W|$ (due to I_S and I_W), exceeds a minimum threshold value. Therefore, the magnitude of I_W is selected to be well above the threshold. Figure 1.4 shows the switching threshold characteristics of a typical MR memory cell. These threshold curves may shift along the x-axis depending on the device size.

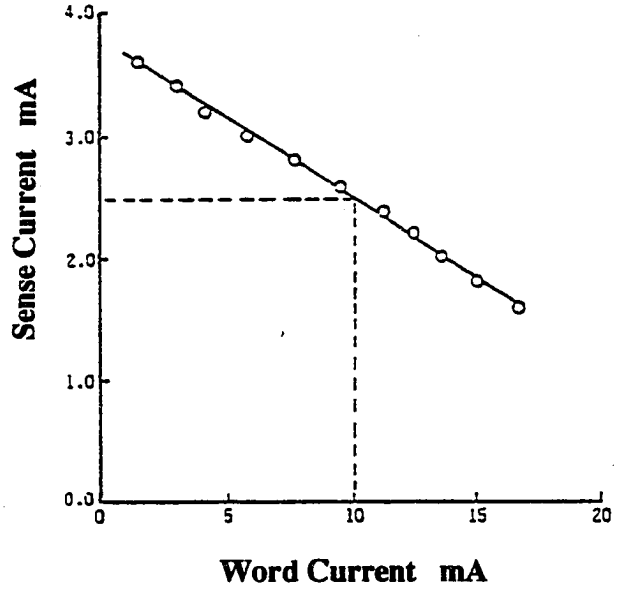


Figure 1.4: Switching Thresholds

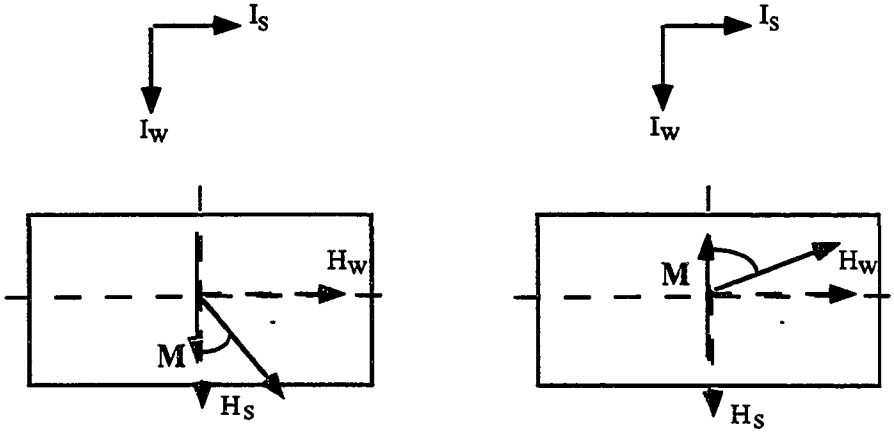
If a positive I_S is applied together with a positive I_W of a magnitude below the threshold, the magnetization vector **M** rotates, and then returns to its original state when I_S and I_W are removed. Thus it is possible to read the stored bit non-destructively. This is called the unipolar read mode since both write and read word currents are in the same direction. A recently discovered, alternative read mode uses a negative word current with the same magnitude as the write word current, to achieve non-destructive readouts with signal levels increased by a factor of four over the original unipolar read mode [7]. This new mode, called the reversed read mode, is preferred since it reduces memory access time and improves the operating margins.

The combinations of sense and word current polarities used for read and write operations in the reversed read mode are shown in Table 1.1.

Figure 1.5 shows the rotation of the magnetization vector (M) during a read. If the cell contains a "1", the sense field (H_S) opposes the stored flux of the bit and the rotation of M is

Table 1.1 The word and sense current polarities for R/W operations

Operation	Word current polarity	Sense current polarity
Write	positive	positive - stores a "0" negative - stores a "1"
Read	negative	positive



Stored '0' Stored '1'

Figure 1.5 : Rotation of Magnetization during a Read

large [2]. If the cell contains a "0", H_S aids the stored flux and the resulting rotation of M is small. Therefore, according to equation (1.1), the resistance of the cell is larger in the former case and smaller in the latter. Thus a "1" can be distinguished from a "0".

The full response of a 1.8x18 μm^2 memory cell for a value of I_S of 3.5 mA is shown in Figure 1.6 [7]. As explained above, the voltage across a cell containing a "1" is higher than that of a cell containing a "0" due to the MR effect. This voltage difference is the output signal (V_{sig}) which is amplified to full logic levels during a read. Since there is no danger of switching when a negative word current is applied, a larger magnitude of word current can be applied in reversed read mode, thus increasing the output signal to about four times that of the unipolar mode. In reversed read mode, V_{sig} (for the current fabrication process) can be approximated by,

$$V_{sig} = \alpha I_S R_S \qquad (1.2)$$

where

I_S = sense current

R_S = cell resistance (along the sense line) = $R_{sh} * L_{cell} / W_{cell}$

α = a process dependent constant which includes C_{MR} as a factor

($\alpha = 0.005$ for the current process)

Typically, the sense current is 3 mA, the word current is 30 mA and the cell sheet resistance R_{sh} is 10 Ω/sq. Thus the sensed signal V_{sig} is directly dependent on the resistance or the aspect ratio (L_{cell} / W_{cell}) of the cell.

Therefore, scaling of dimensions doesn't affect the signal level as long as the cell aspect ratio is maintained. This is a remarkable property of MRAM cells which favours high

density memories, possibly at the lithographic limit. On the other hand, it is possible to increase the output signal by increasing the cell aspect ratio, in order to design faster memories at lower densities. It has been shown that it is possible to design MRAMs with access time in the range of 10-35 ns at a bit density of 0.25 Mbits/cm^2 [13].

1.3 Memory Cell Organization and Fabrication

In a MRAM, the memory cells are organized in a 2-D array with the sense lines and word lines providing random accessibility. This organization also makes provision for sharing the support electronics among memory cells (Figure 1.7).

Fabrication of these devices can be easily implemented using conventional semiconductor processes [2]. Figure 1.8 shows the cross section of a memory cell [7]. During fabrication, the memory cells are laid out on an integrated circuit wafer, fabricated up through and including contact cuts to the underlying transistors [2]. Therefore, it is possible to bury some of the support electronics and minimize chip area.

The first step in the fabrication process is the deposition of the magnetic sandwich and the first metal layer. This is typically done using conventional sputtering deposition techniques. The first metal and the magnetic sandwich are then etched to form the sense lines. Next the first metal is etched away from the areas where cells are desired. This leaves first metal for connections to other cells on a sense line (shorting bars) and for the other on-chip electronics. Then, an insulating layer is deposited, and vias are etched where needed in the circuitry. Finally, the second level metal is deposited and etched to form word lines and interconnections to the on chip electronics (Figure 1.8).

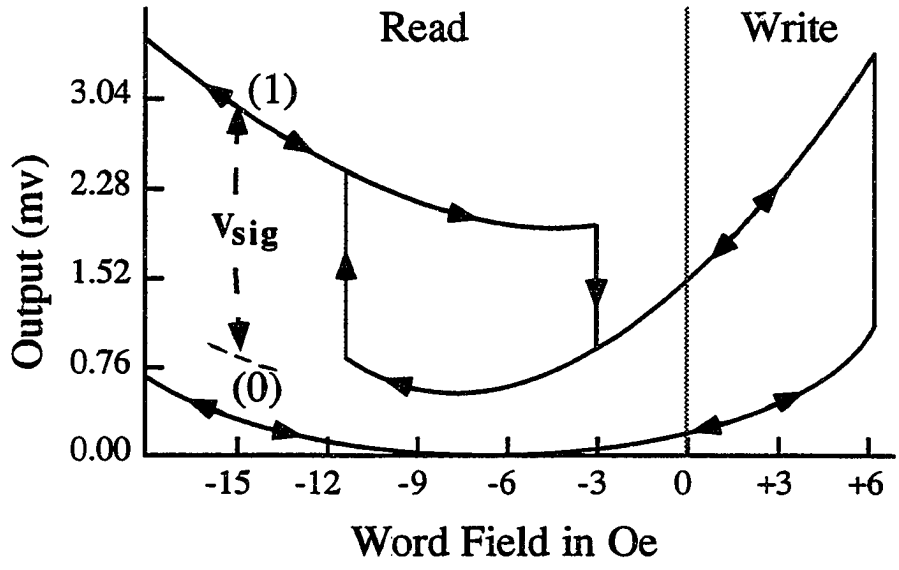


Figure 1.6 : Typical Memory Cell Response

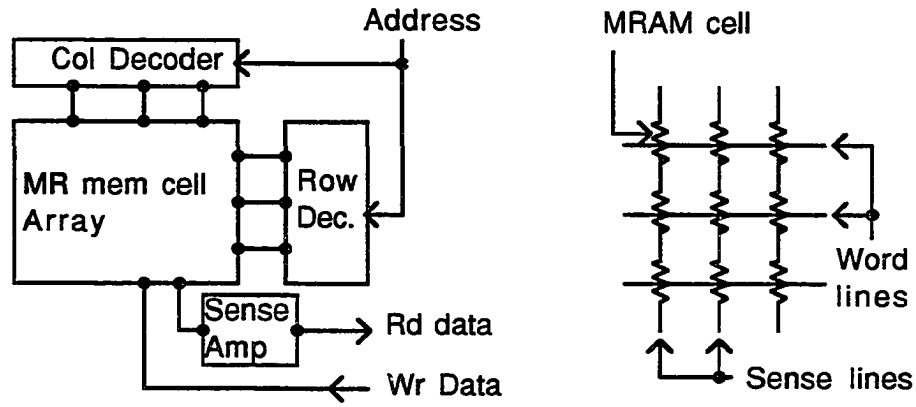


Figure 1.7 : Memory Cell Array Structure

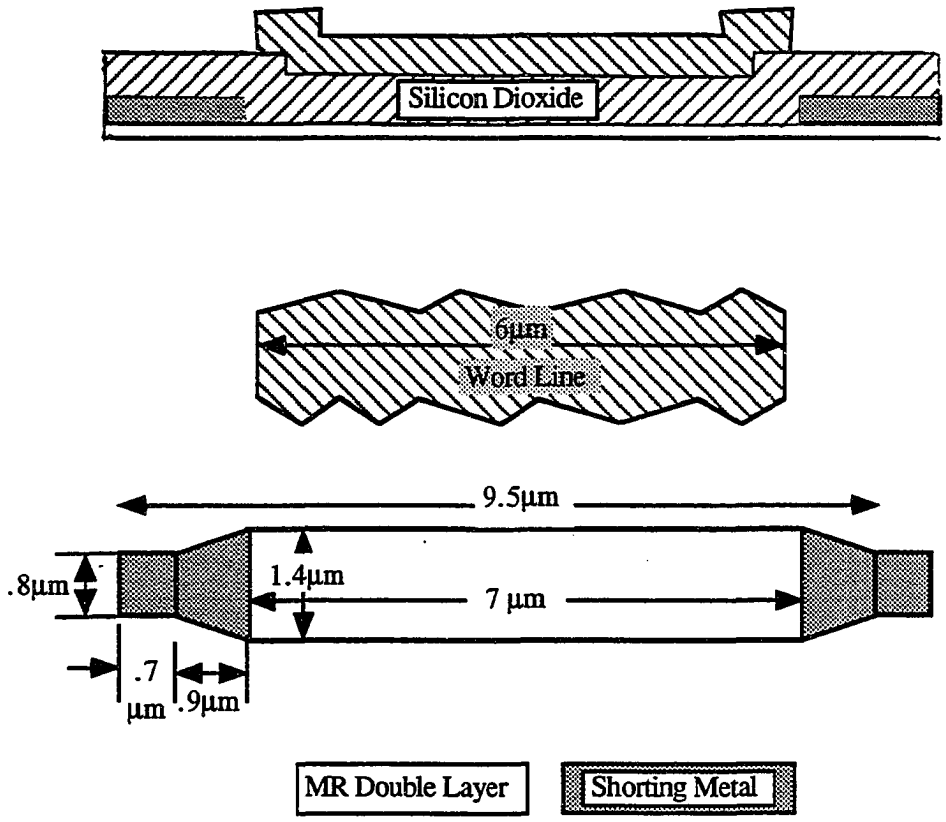


Figure 1.8 : Cell Cross-section and Top View

Therefore, in a standard CMOS process, only one additional mask is needed to fabricate MRAMs. This is a definite advantage over DRAMs which typically use 18 masks, and implies comparatively low production costs in a mass scale production environment.

1.4 Properties of MRAMs

The key desirable properties of MRAMs are summarized below.

(1) Nonvolatile - These memories do not require refreshing and do not lose the contents when power is removed. Therefore, the average power consumption is quite low.

(2) Radiation Hard - The magnetic nature of the storage cells makes these memories radiation hard and therefore suitable for space and military applications.

(3) Unlimited writes with no wear-out phenomena -
Write stability tests performed on 2x20 μm^2 memory cells by subjecting them to a total of $2.0x10^{15}$ write operations (at 60 MHz for 15 months) has shown the cell behavior to be similar to plated wire or magnetic core cells, with no wear-out phenomena as in the case of ferro-electric cells [8].

(4) Non-destructive readout

(5) Random Accessibility

(6) Low cost processing with typically one mask beyond a standard CMOS process

(7) Logic level compatibility with single 5V supply

(8) High Densities - Cells do not have contacts and share the support electronics. It is also possible to scale the cell size without loss of signal.

(9) Range of possible access times -

Studies have shown that a write operation can be completed within a few nanoseconds [14]. The speed density trade-off governs the cell size needed to meet a specific read time, and it is possible to achieve access times as low as 10-35 ns (15x25 μm^2/bit) [12] or as high as 3 μs with unipolar read (8.5x9.5 mm^2/Mbit) [6].

Thus it can be seen that these memories are suitable for a wide range of memory applications, from disc caches to high speed RAMs.

1.5 MRAM and the Computer Memory Spectrum

Today, the computer systems place an enormous demand on the speed and capacity of their memory subsystems in order to achieve high performance. In fact, the major portion of the computer hardware market is on memories ranging from semiconductor memories to hard disks and tapes. Fast memories are more expensive than the slow ones as shown by the "Cost vs Access time Relation of Memory Technologies" in Figure 1.9 [5]. To be commercially successful, memories need to fit on the technology curve which is a moving target that produces an approximately 25% reduction of price every year. There exists a clear gap on the technology curve between DRAMs and disc drives, with no cost-effective memory technology in the 200ns - 10ms access time range. A memory technology which can fit in that gap would be very useful for the performance enhancement of computer systems.

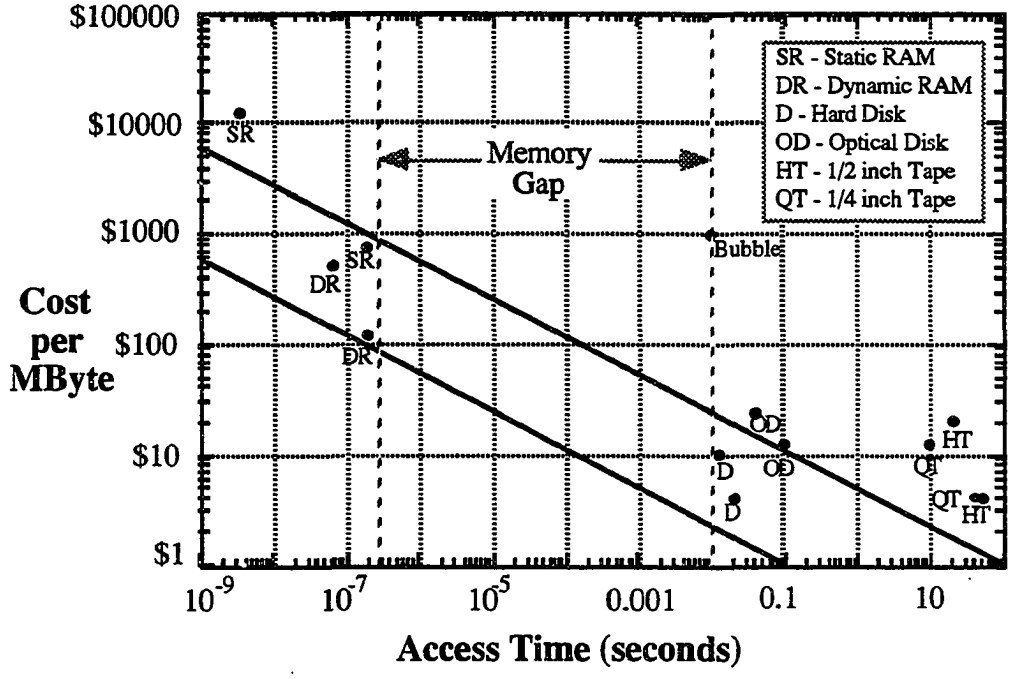


Figure 1.9 : Cost vs Access Times for Current Memory Technologies

It is possible to reduce the cost of MRAMs by increasing the density at the expense of speed. Therefore, it has the potential to fit in the gap between DRAMs and disks on the Technology curve. Such a memory fabricated using wafer scale integration would be very well suited for disk caches [2].

At present, DRAMs have reached a density of 16 Mbits in 75 mm^2 with an access time of 200 ns. The MRAM design presented here achieves a density of 1 Mbit in 50 mm^2 with an access time of 800 ns/byte. A newly discovered phenomena called the Giant Magnetoresistive (GMR) effect which increases the signal by a factor of 7.5, implies the

possibility of increasing the speed as well as the density of MRAMs. Therefore, it is also possible for MRAMs with GMR bits to compete with DRAMs for the computer main memory market. MRAMs will have the added advantage of a low number of mask levels, nonvolatility and no soft-error sensitivity over DRAMs.

Today, nonvolatile programmable memories such as EPROMs, EEPROMs and Flash memories also play an important part in system design, with applications in microcontrollers, remote battery powered systems, flight data recorders and communication equipment where parameters often change to accommodate different formats.

EPROMs offer bit densities as high as 1M, read times between 100 -200 ns, but must be taken off-line to be erased with UV light prior to reprogramming and allows a maximum of 100 write cycles [4]. Therefore, the write time for an EPROM can take well up to 20 minutes. EEPROMs are easily reprogrammable, typically with 160 μs/byte write time, 120 ns read time, 256 Kbit density, and allow a maximum of 10^5 write cycles. Flash memories are expected to fill a niche between conventional EPROMs and EEPROMs by offering the former's density and the latter's reprogramming convenience. A typical flash memory has 1 Mbit density, 200 ns access time, 525 μs/byte write time, but can support only a maximum of 10^4 write cycles.

It has been shown that the MRAMs can achieve speeds as high as 35 ns with a density of 256 Kbits/cm^2 [12]. With GMR bits, the density is expected to increase by 50% for the same speed. Therefore, MRAMs are better suited for nonvolatile programmable memory applications.

SRAMs are very high speed memories with typical access times of 5 - 10 ns in ECL and 20 -50 ns in CMOS. The memory cell has 4 to 6 transistors and no refresh requirement. The high cost limits SRAM applications to high speed caches and registers. Battery backed SRAMs are often used to retain critical data at the event of a power loss. High speed

MRAMs will be a better alternative to battery backed SRAMs which tend to be quite bulky. Also, MRAMs can be used instead of SRAMs in programmable logic devices (PLDs), where SRAMs are used for storage of PLD configurations [10].

Last but not least, MRAMs are the best technology to replace plated wire memories in military and aerospace applications since they were designed for that purpose.

1.6 State of the Art and Research Trends in MRAMs

MRAM technology has shown rapid development in the past few years. A considerable amount of more work is needed to ensure the ability of this technology to keep up with the developments in the semiconductor industry and be commercially viable in the global memory market.

Honeywell Corp. is currently producing 16 Kbit MRAM chips. This uses a triple redundant cell which has 3 memory elements (each of 60 Ω with a C_{MR} of 2-2.5%) to achieve sufficient reliability. The nominal sense signal is 3 mV. A "current mode" sensing scheme which uses tightly controlled sense current sources, and compares the accessed element output with that from a duplicate 'ping-pong' matching array to determine the state of a bit, is implemented on this chip. Some key parameters are: $I_S = 3.5$ mA, I_W(read) = 45 mA, I_W(write) = 30 mA, and the output resistance of the current source $R_{out} = 10$ kΩ. ["Current mode" sensing is described in Chapter 2.]

There are three main research areas which are being pursued at present.

1. Yield Enhancement and Defect Analysis -

   It is very important to identify possible defects and failure mechanisms and their relation to the manufacturing process in order to improve the yield and reliability. Several

discoveries made within the past year or so have improved the expected yield to 1 bad bit in 1000 to 10,000.

2. Higher Magnetoresistance -

Researchers at IBM and NVE have found that it is possible to improve the MR coefficient of materials using the 'spin valve' effect (GMR materials). NVE has produced materials with a MR coefficient of 6% which is three times that of permalloy. An increased C_{MR} produces a proportional increase in the sense signal which can be used to improve the read access time and achieve higher density. It is also expected the spin valve materials will have higher values of R_{sh} (approximately 25Ω) which would result in much lower cell aspect ratios and therefore, higher cell density.

3. Sensing Scheme and Cell Design for High Densities -

In typical MRAMs designed so far, the on chip support electronics occupy more than 50% of the chip area. It is essential to improve the density of support circuits as well as the memory cells in order for MRAMs to achieve a higher density than the DRAMs. The existing sensing schemes are not designed for such high densities and therefore, a new technique is required. The work being done at Iowa State University on "1 Mbit MRAM" falls into this category.

1.7 1 Mbit MRAM Project Overview

The research effort at Iowa State University was focussed on circuit densification and sensing issues involving both elements and electronics, which were implemented using a 1Mbit MRAM design with the following specifications.

Memory Size	1 Mbit
Chip Area	0.5 cm^2 @ minimum feature of 0.8 μm
% MR cell area	> 50% of the chip area
Byte read time	< 1 μs (with all 8 bits read in parallel)
Yield	90% with a failure rate of 1/4000

Among the contributions are an improved logical organization of bit arrays with buried transistors, redundancy schemes [3], and a new sensing technique which uses voltage mode small signal sensing and self referencing [11] to improve the density and accommodate future low voltage operation.

This thesis presents the work done in the development of a new voltage mode sensing technique and the design of the low noise front end of the very small signal sensing scheme.

CHAPTER 2. SENSING MODES

All MRAMs that have been fabricated so far use current mode sensing. Voltage mode is a new alternative that is being investigated using the 1 Mbit MRAM design.

2.1 Current Mode Sensing

In current mode sensing (Figure 2.1), a tightly controlled constant current source is used to supply the sense current through the memory cell. The switching transistors T_{pp}, T_{nn}, T_{pn} and T_{np} determine the direction of current. A current source and the switching transistor pairs are shared by multiple sense lines, each with multiple sense elements. A sense line is selected by turning on the corresponding gate transistor. The cell output signal is sensed at point X. Since the applied sense current is a well controlled constant, any changes in the element resistance is reflected on the sense point voltage (V_X) which is then taken to the sense amplifier. Since the output impedance of the current source is much larger than the equivalent resistance of the 'on' transistors and the memory cells on a sense line, a large percentage of the signal appears at the sense point. This is typically in the range of 85% - 95% [1].

In order to maintain a sufficient Signal to Noise Ratio (SNR), the output of a cell is sensed with respect to that of a dummy cell, and it is necessary to use a separate current source to power up the dummy.

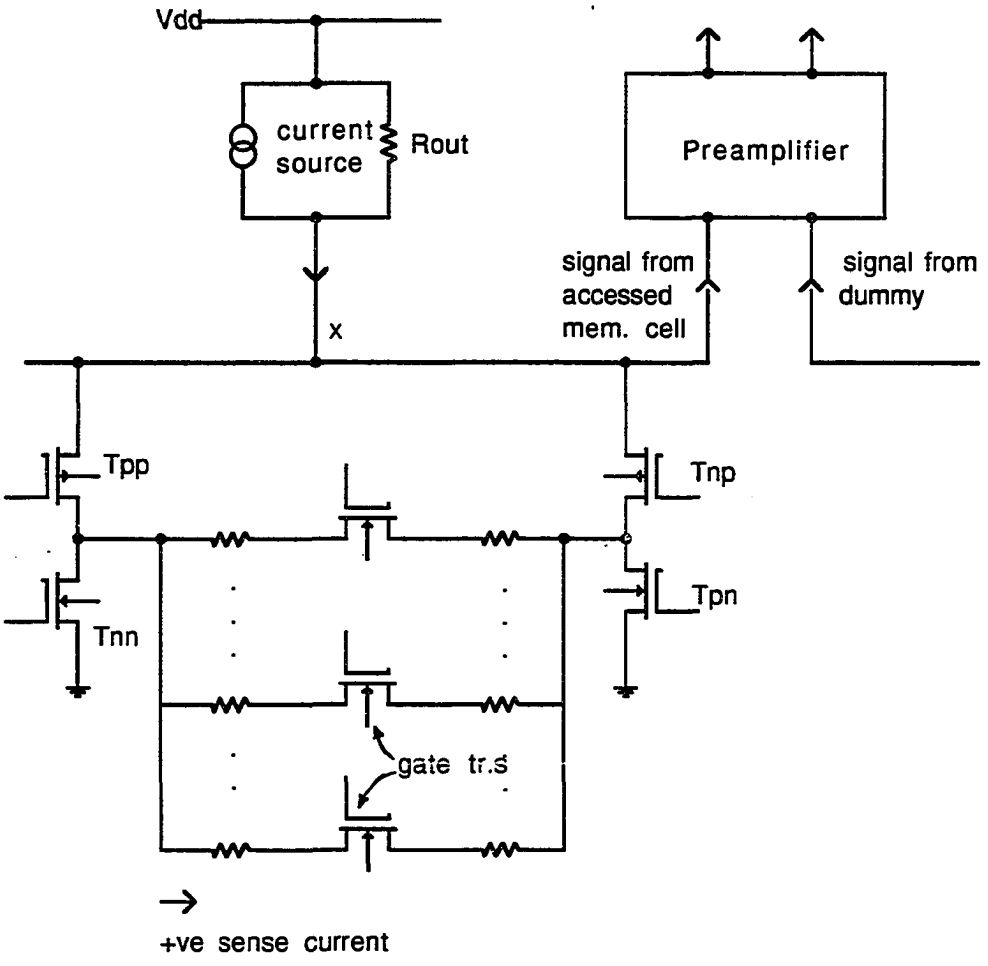


Figure 2.1 : Current Mode Sensing

In the "ping-pong" scheme, each memory cell has its own dummy cell and effectively 2 memory cells are used to store a data bit. i.e., the cell where the bit is stored and the corresponding dummy cell where the complement of the bit is stored. This achieves a higher signal to noise ratio by doubling the signal, at the cost of increased cell area.

2.2 Voltage Mode Sensing

Voltage mode sensing eliminates the tightly controlled current source (Figure 2.2). Instead, the supply voltage (V_{DD}) is temperature compensated to maintain the sense current at its nominal value. The transistor pairs T_{pp}, T_{nn}, T_{pn} and T_{np} perform the dual functions of supplying the sense current and controlling its direction. The gate transistor selects the sense line, and a mux transistor is used to transmit the signal that reflects the change in element resistance to the sense amplifier. The optimal signal level is at the mid point of the sense line and 50% of the cell output signal appears here. This is called mid-line sensing.

The dummy line is in the same sense line array and shares the switching transistor pairs, with the accessed sense line to power up.

2.3 A Comparison of Current Mode and Voltage Mode

For a fair comparison, both the current mode (CM) and voltage mode (VM) need to be analyzed under similar conditions. Therefore, two basic designs, each done to achieve the same cell array area were used for the comparison.

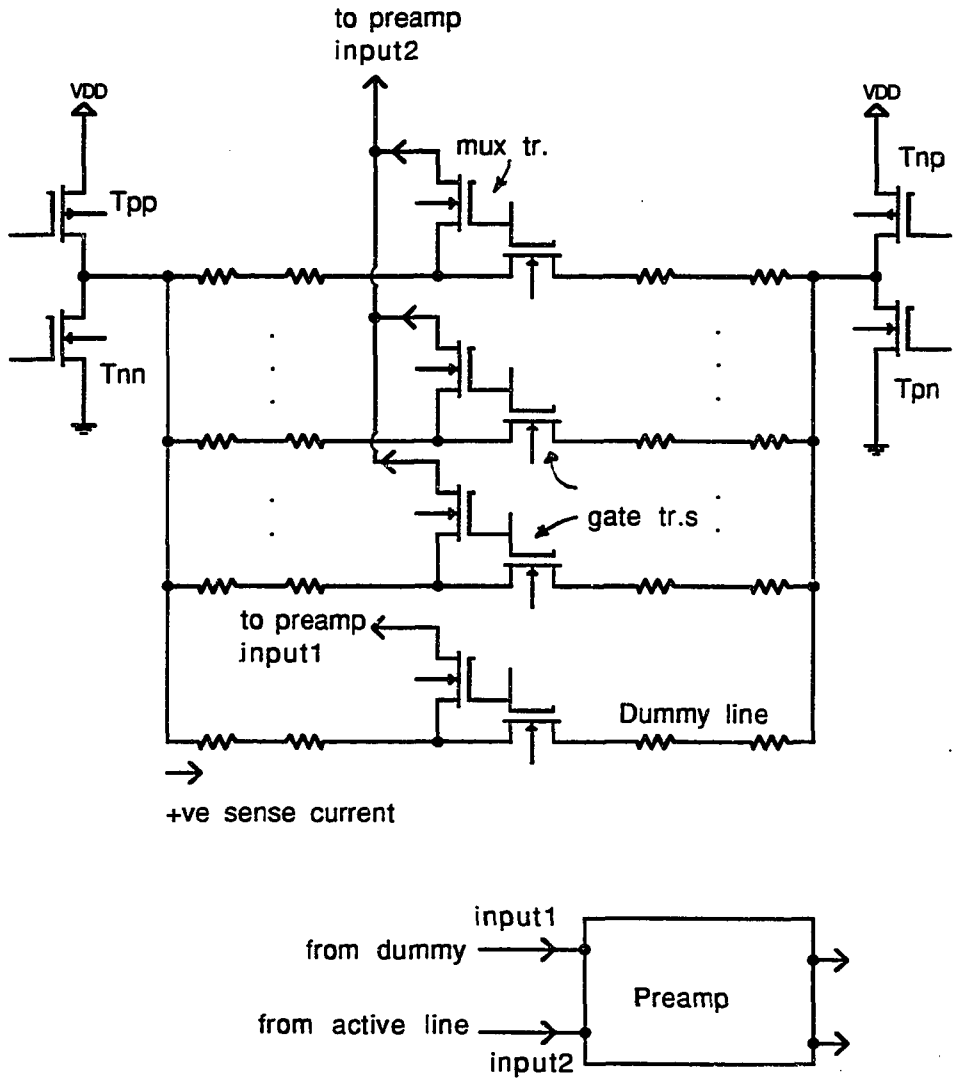


Figure 2.2 : Voltage Mode Sensing

2.3.1 Cell Size Determination

Figure 2.3 shows the memory element used in the designs for a 0.8 micron process. Its effective resistance is given by,

$$R_{elt} = R_{sh} * L_{elt} / W_{elt} + R_c \qquad (2.1)$$

where R_c is the contact resistance in the taper which is approximately 10 Ω (Figure 2.3).

For the voltage mode design, an element with $L_{elt} = 7$ μm and $W_{elt} = 1.4$ μm was selected.

$\therefore$ R_{elt} (VM) = 60 Ω

No. of elements per sense line in VM = 16

Therefore, in voltage mode, the estimated length of a sense line, L_s (≡ the length of memory cell array) is given by,

$$L_s (VM) = 16*(L_{elt}+L_{tap}) + ACD + AGM \qquad (2.2)$$

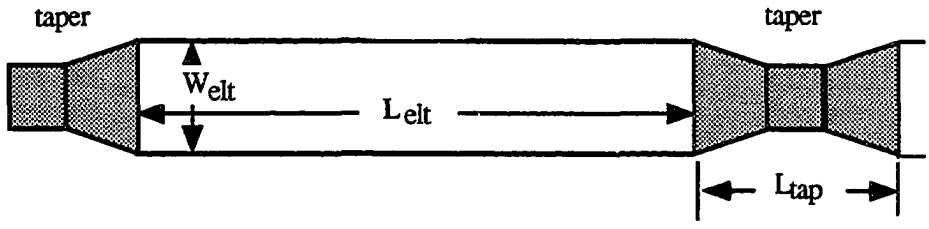


Figure 2.3 : Memory Cell Dimensions

where ACD is the allowance for central decoding (16 μm) and AGM is the allowance for gate and mux transistor contacts (32 μm).

$\therefore$ L_s (VM) = 208 μm

The element size for the current mode design was determined as follows :

No. of elements per sense line in CM = 8

Therefore, the number of sense lines in the current mode design is twice that of the voltage mode design. Thus, in order to keep the cell array areas the same, the sense line lengths in the current mode should be halved.

$\therefore$ L_s (CM) = 104 μm

And in CM design AGM reduces to 24 μm since there are no mux transistors.

$\therefore$ $L_{elt}+L_{tap}$ = 8 μm in CM

and R_{elt} (CM) = 45 Ω

2.3.2 Estimation of Equivalent Noise Resistances

The switching transistors operate in the Ohmic region. The equivalent noise resistance of an Ohmic transistor is its dc resistance given by

$$R_{dc} = V_{ds}/I_{ds} = \{K*W/L\,(V_{gs} - V_t - V_{ds}/2)\}^{-1} \qquad (2.3)$$

The gate and mux transistors are sized so that they can be buried under the magnetic elements in the sense lines (Figure 2.4). Even though they operate in the Ohmic region, the equivalent resistances cannot be accurately modeled using equation 2.3 since it does not account for source and drain spreading resistances. Therefore, a distributed resistive ladder

network approach is used to determine the equivalent resistances as explained in Section 2.3.4.

In current mode design, the current source transistor is operating in saturation and its equivalent noise current is given by

$$i_{ndt} = \text{sqrt}\{ 8kT\, g_m /3\} \quad (2.4)$$

where

$$g_m = K*W/L\, (V_{gs} - V_t) \quad (2.5)$$

A differential preamplifier with an equivalent noise resistance (R_{nt}) of 125 Ω at each input gate is assumed for both designs. It is also assumed that the output of the accessed sense element is sensed relative to that of a shared dummy element which has a bit '0' stored in it.

The effects of heating and scaling of dimensions on the equivalent noise resistances, are discussed in Section 2.3.5. These effects are reflected in the noise resistances and noise currents computed in Sections 2.3.6 and 2.3.7.

2.3.4 Gate and Mux Transistor Modeling

The layout and the dimensions of the gate and mux transistors together with the corresponding circuit models are shown in Figure 2.5.

The current flow from the drain to source in the gate transistor takes place as shown in Figure 2.6(a). Therefore, the gate transistor can be modeled as a distributed resistive ladder network as shown in Figure 2.6(b). There, r_p is the channel resistance per unit width of channel and $r_s/2$ is the diffusion resistance per unit width of the transistor along the drain or source.

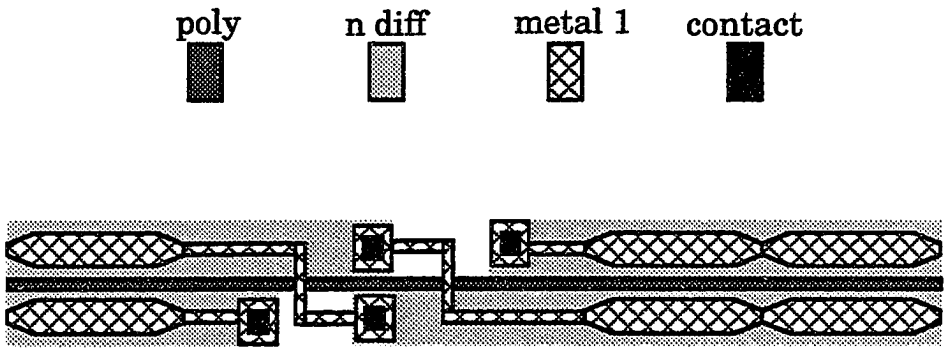


Figure 2.4 : Buried Gate and Mux Transistor Layouts

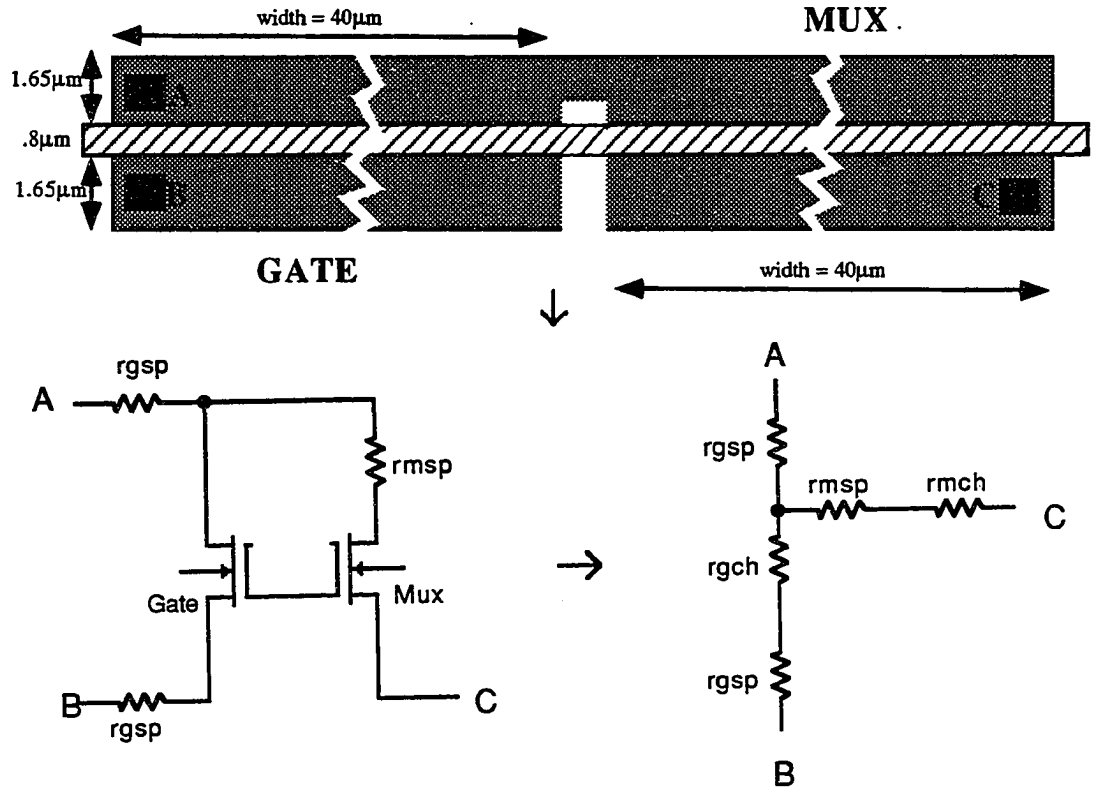
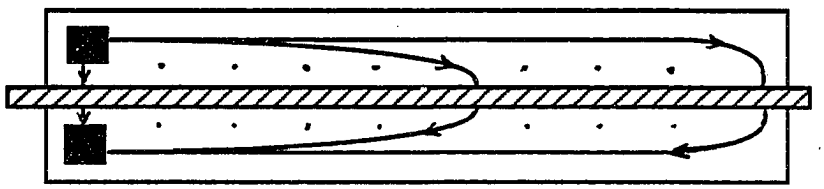
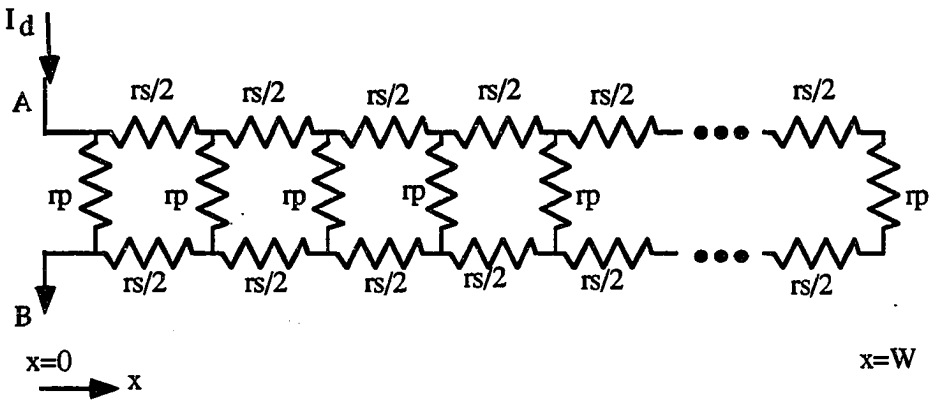


Figure 2.5 : Mux and Gate Transistor Dimensions with Equivalent Resistances



(a)



(b)

Figure 2.6 : Modeling of Gate Transistor

$\therefore\ r_p = R_{dc} * W\ \Omega\mu m$

where R_{dc} is as defined in eq. (2.3)

and $r_s/2 = R_{sh(n\text{-}diffusion)} / d\ \Omega/\mu m$

with $R_{sh(n\text{-}diffusion)} = 3.03\ \Omega/sq$ for the current process.

The voltages and currents in the network are given by,

$$DV(x) = -r_s I(x) \tag{2.6}$$

$$DI(x) = -V(x)/r_p \tag{2.7}$$

using D operators. The above two equations can be combined to form

$$D^2I - (r_s/r_p) I = 0 \tag{2.8}$$

$$D^2V - (r_s/r_p) V = 0 \tag{2.9}$$

which has roots +/-α where α = sqrt (r_s/r_p).

Therefore, the solutions are in the form

$$I(x) = Ae^{\alpha x} + Be^{-\alpha x} \tag{2.10}$$

$$V(x) = Pe^{\alpha x} + Qe^{-\alpha x} \tag{2.11}$$

Using the boundary condition at x = W where current goes to zero (at the end of the transistor),

$I(W) = 0 \quad \Rightarrow \quad A = -Be^{-2\alpha W}$

The total current through the transistor, I_d is given by,

$I_d = I(0) = A + B = B(1- e^{-2\alpha W}) \quad \Rightarrow \quad B = Id(1-e^{-2\alpha W})^{-1}$

From equation (2.6),

$$Pe^{\alpha x} - Q\alpha e^{-\alpha x} = - r_s Ae^{\alpha x} - r_s Be^{-\alpha x}$$

Since the above relation should be true for all x,

$$P= -r_s A/\alpha \quad \text{and} \quad Q = r_s B/\alpha$$

Therefore, the solutions are in the form,

$$I(x) = Be^{-\alpha x} \left[1 - e^{-2\alpha(W-x)} \right] \quad (2.12)$$

$$V(x) = B (r_s/\alpha) \left[e^{-\alpha x} + e^{-2\alpha W} \right] \quad (2.13)$$

The equivalent resistance of the transistor is given by V(x)/I(x) at x=0.

$\therefore R_{eq} = (r_s r_p)^{0.5} (1 + e^{-2\alpha W}) / (1 - e^{-2\alpha W})$

$r_{ch} = V(W)/I_d = (r_s r_p)^{0.5} 2e^{-\alpha W} / (1 - e^{-2\alpha W})$

Therefore, the spreading resistance component can be found using,

$R_{eq} = 2r_{sp} + r_{ch}$

and the total noise resistance of the transistor is R_{eq}.

In the mux transistor, the spreading resistance component is equivalent to that of the source (or drain).

$\therefore r_{sp} = R_{sh(n\text{-}diffusion)} * W$

r_{ch} is the dc resistance of the transistor which can be found using equation (2.3). Thus, the equivalent resistance of the mux transistor is given by

$R_{eq} = r_{sp} + r_{ch}$

Therefore, the equivalent resistance of the mux transistor tends to be higher than that of the gate transistor.

2.3.5 Effects of Heating and Scaling on Noise Resistances

The effect of elevated temperatures on the sense element resistance is calculated using

$$R_{elt} = R_o (1 + \alpha \Delta t) \quad (2.14)$$

where α = thermal coefficient of MR elements = 0.0015 / °C.

In a MOS transistor, the temperature dependance of the transconductance parameter K is given by ,

$$K(T_1) = (T_0/T_1)^{1.5} * K(T_0) \qquad (2.15)$$

where T_1 and T_0 are in Kelvin. To a first order approximation, the temperature dependence of dc resistance (R_{dc}) in a MOS transistor is governed by that of K.

Shrinking dimensions result in similar scaling of V_{DD}, currents and gate oxide thickness t_{ox}. Since $K = \mu C_{ox}$, K increases proportionately.

2.3.6 SNR Calculation for the VM Design

The estimated bandwidth of the system is 1-5 MHz and therefore the major contribution to system noise is from thermal noise. A schematic of a sense line and the corresponding noise resistances are given in Figure 2.7. Table 2.1 shows how these noise resistances vary with the operating temperature and supply voltage.

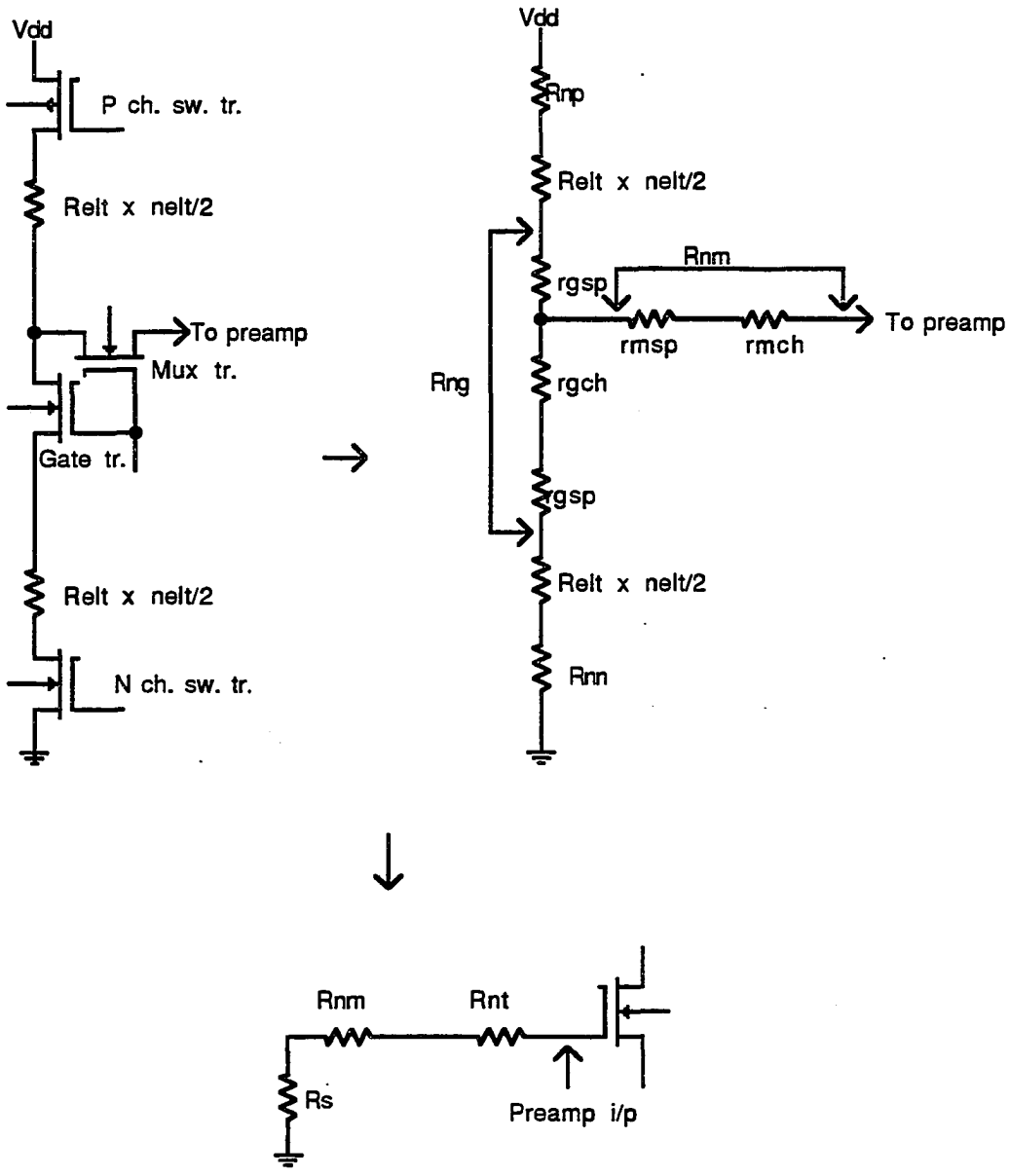
The total noise voltage at the input to the preamplifier is given by

$$v_{noise} = \text{sqrt} \{ 2 * 4kT\Delta f (R_{ns} + R_{nmux} + R_{nt}) \} \qquad (2.16)$$

where R_{nt} is the noise resistance of the preamplifier referred to the input.

The output signal for mid-line sensing is given by ,

$$V_{sig} = 0.0025 R_{elt} I_s \qquad (2.17)$$



$$Rs = (Rnp + Relt \times nelt/2 + rgsp) \;//\; (rgch + rgsp + Relt \times nelt/2 + Rnn)$$

Figure 2.7 : Equivalent Noise Resistances in Voltage Mode

Table 2.1 Equivalent Noise Resistances for VM Design

temp(C)	VDD	Rnp	Relt	$n_{elt/line}$	Rng	Rnn	Rnmux	Rnt
25	3.9	100	60.0	16	116	70	151.7	125
75	4.3	126	64.5	16	141	88.2	180.17	157.5
100	4.5	140	66.75	16	154.8	98	199.6	175
25	2.3	100	60	12	130.4	70	173.59	125
75	2.6	126	64.5	12	159.6	88.2	217.1	157.5
100	2.7	140	66.75	12	176.8	98	240.9	175

The supply voltage V_{DD} is temperature compensated to maintain a constant sense current.

2.3.7 SNR Calculation for the CM Design

A schematic of a CM sense line and corresponding noise resistances at room temperature are shown in Figure 2.8. Table 2.2 shows how the noise resistances and noise currents vary with the operating temperature and supply voltage.

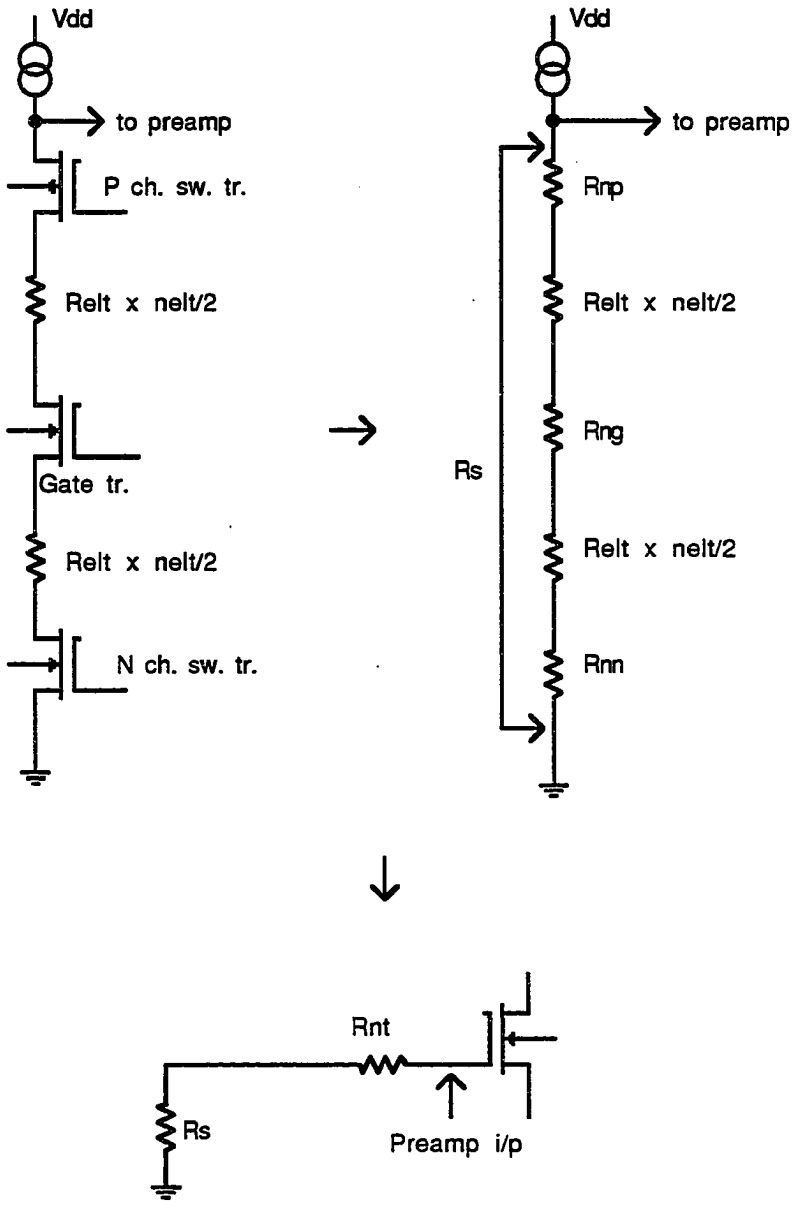
There are 2 dominant noise sources.

(1) The thermal noise generated by the sense line and the input stage of the preamplifier, which is given by,

$$v_{n1} = \text{sqrt}\ \{2^* 4kT\Delta f\ (R_{ns} + R_{nt})\ \} \qquad (2.18)$$

(2) The effect of the thermal noise generated in each current source can be found using,

$$v_{n2} = \text{sqrt}\ \{8/3 * 4kT\Delta f\ g_m^* R_{ns}\} \qquad (2.19)$$



$$Rs = (Rnp + Relt \times nelt + Rng + Rnn)$$

Figure 2.8 : Equivalent Noise Resistances in Current Mode

Table 2.2 Equivalent Noise Resistances and currents for CM Design

temp (C)	VDD	Rnp	Relt	n_{elt} /line	Rng	Rnn	i_{dnt}(nA)	Rnt
25	4.5	100	45	8	99.7	70	12.04	125
75	4.5	126	48.375	8	117.7	88.2	13.67	157.5
100	4.5	140	50.0625	8	127.7	98	14.56	175
25	2.7	100	45	6	110	70	13.47	125
75	2.7	126	48.375	6	131.3	88.2	15.8	157.5
100	2.7	140	50.0625	6	142	98	16.58	175

where $g_m = \text{sqrt}\{2K * W/L * I_S\}$

and $K*W/L = 2*I_S / (V_{gs} - V_t)^2$

To maintain the current source in saturation with a safety margin (SM), the gate voltage should be set according to,

$$(V_{gs} - V_t)_{max} = V_{DD} - I_S R_{ns} - SM$$

Since there are 2 current sources powering the accessed sense line and the dummy, the total noise voltage at the input to the preamplifier is given by,

$$v_{noise} = \text{sqrt}\{ (v_{n1})^2 + 2*(v_{n2})^2 \} \qquad (2.20)$$

A reasonable estimate for the output signal for current mode sensing is 95% of the bit output signal which is given by,

$$V_{sig} = 0.00475\ R_{elt}\ I_s \qquad (2.21)$$

2.3.8 Results and Conclusions

First a nominal supply voltage of 5V was assumed, and the SNR estimations for several temperatures ranging from 0 °C to 100 °C were done for both modes. Since the voltage mode depends on a temperature compensated voltage supply, V_{DD} was varied from 3.7V to 4.5V over the temperature range. In the current mode design V_{DD} was set to 4.5V and the safety margin to maintain the current source in saturation (SM) was set to 0.15V. A charge pumped 6V supply was assumed for the gate voltages of the mux and gate transistors and the nominal sense current was set to 3 mA.

Then the above procedure was repeated for a nominal supply voltage of 3V. In this case, the temperature compensated supply voltage was varied from 2.2V to 2.7V over the temperature range. In current mode design, V_{DD} was set to 2.7V and SM was reduced to 0.1V. The gate voltage for the mux and gate transistors were charge pumped up to 3.6V and the nominal sense current was reduced to 2.2 mA.

The results obtained (Table 2.3) indicate that the voltage mode has a superior SNR for the same cell array sizes.

The current source needs to have a very high output resistance to keep the sense current constant irrespective of the voltage across it. A current source is implemented with MOS transistors in saturation and this requires a large voltage drop across the current source (typically, about 2V including safety margins). This restricts the number of memory cells that can be strung on a single sense line. Studies have shown that optimal performance can be achieved when approximately $0.5V_{DD}$ is applied across the memory cells. As the supply

Table 2.3 Signal to Noise Ratios for VM & CM

Temp (C)	VDD (CM)	VDD (VM)	Is (mA)	SNR (CM)	SNR(VM)
25	4.5	3.9	3.13	43.2	46.69
75	4.5	4.3	3.10	34.9	39.5
100	4.5	4.5	3.08	31.3	35.65
25	2.7	2.3	2.25	31.8	34
75	2.7	2.6	2.26	25.6	28.58
100	2.7	2.7	2.20	22.6	25.8

levels reduce, the voltage across the current source decreases resulting in increased noise levels.

On the other hand, voltage mode sensing doesn't require the use of a current source, and therefore, can support more cells on a sense line. Typically, this is double that of the current mode scheme.

The sizes of the switching transistors are comparable in both modes for a given sense current. Since the current mode design has twice the number of sense lines as in the voltage mode, the number of switching transistor pairs too need to be doubled. Therefore, per cell support circuit area overhead taken up by these transistors is higher in current mode sensing and it further increases due to the current source. (Both the gate and mux transistors are buried under the sense lines and therefore do not contribute much to the overhead.)

Therefore, it can be seen that the proposed voltage mode sense technique achieves superior performance with higher SNRs and densities.

CHAPTER 3. DEVELOPMENT OF THE FRONT END SENSING SCHEME AND ITS SPECIFICATIONS

3.1 Design Approach and Organization of the 1 Mbit Memory

The main design goals of this project are ,

1. Memory size - 1 Mbit
2. Chip area - 0.5 cm^2 @ minimum feature size of 0.8 μm
3. To limit the area occupied by the support electronics to be less than 50% of chip area
4. Byte read time < 1 μs (Block oriented memory with 8 bits read in parallel)
5. Yield - 90% with a failure rate of 1/4000

It is necessary to eliminate the duplicate "ping pong" array used to cancel the unwanted coupling in early designs, in order to achieve the target density. This is done by going into a new "self referencing" scheme which reduces the cell array area by a factor of 2 by eliminating the ping pong matching array [11]. In effect, it compares a bit 'zero' signal with a bit 'one' signal obtained from the same memory cell. First, the cell output is sensed with a positive sense current and this signal is sampled and held in a capacitor. Next, the sense current is reversed and the cell output which now corresponds to the inverse of the stored bit, is sensed and compared with the first sample. The result of this comparison is either

positive going or negative going depending on the state of the bit and it can be amplified to give the corresponding logic output.

Area occupied by the support electronics can be considerably reduced by burying the gate and mux transistors under the sense lines. Therefore, the gate and mux transistors are sized to fit underneath a sense line [3]. Sparing techniques are used to improve the yield.

The cell size which depends on the target die area determines the signal level. Voltage mode sensing is selected to achieve a better signal to noise performance, and therefore, lower access time.

Figure 3.1 shows the organization of the 1 Mbit memory chip. This memory is divided into 32 "double chunks" with one spare double chunk. Each double chunk consists of 8 "data segments". A data segment contains 256 regular sense lines with 16 elements/line, and spare sense lines [3].

Each data segment is powered up by its own drive transistors (switching transistors). During a read operation, each bit of a byte comes from the 8 segments on a double chunk.

A word line runs over the entire length of a double chunk, i.e., 2048 sense lines. The word drive transistor pairs are shared by 128 word lines.

sense line pitch = 3μm

word line pitch = 13μm

3.2 Cell Size and Signal Levels

Target area for a 1 Mbit = 0.5 cm^2

Area occupied by the memory cell array = 0.25 cm^2

$\therefore$ Area / memory cell = 25 μm^2

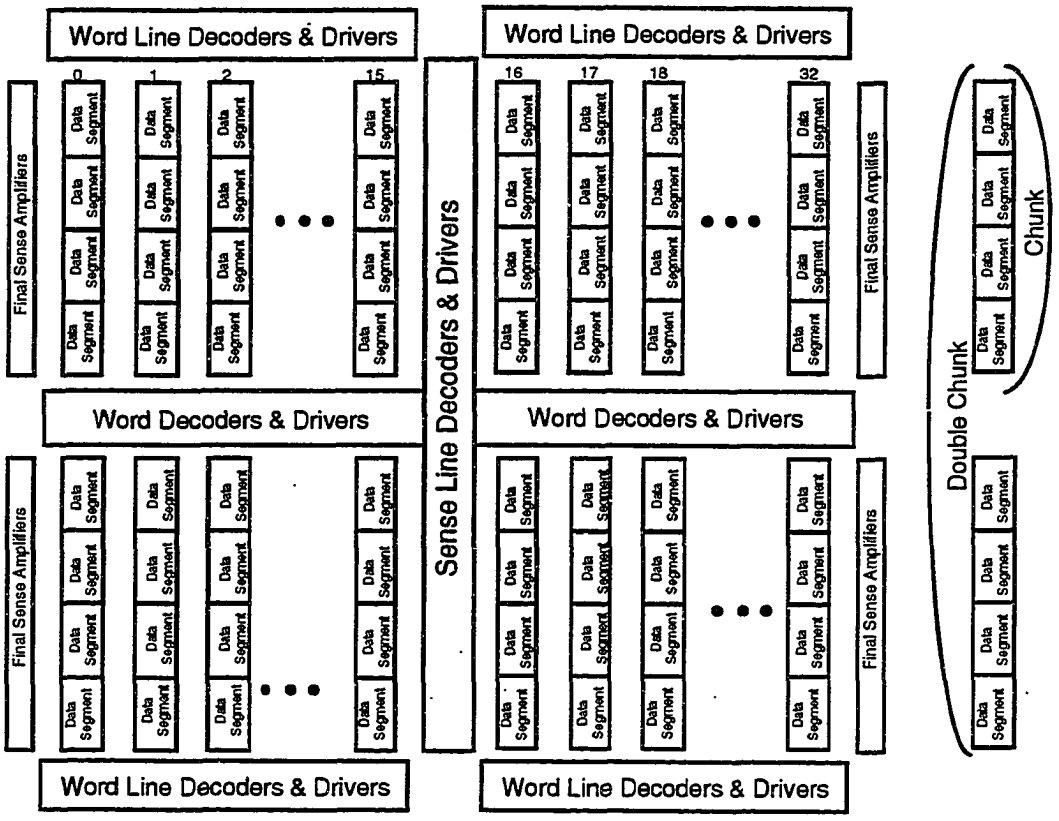


Figure 3.1 : Organization of 1 Mbit MRAM Chip

Therefore, a 1.4x7 μm^2 memory element with a 2.5 µm taper which occupies an area of 24.7 μm^2 is selected for this design (Figure 3.2).

The nominal supply voltage is 5V and the operating temperature range is 0°C to 75°C. The voltage supply is temperature compensated to keep the sense current (I_S) steady at 3 mA through out the operating temperature range. The word current (I_W) is set to 30 mA.

$R_{elt} = R_{sh} * 7/1.4 + 10 = 60\ \Omega$

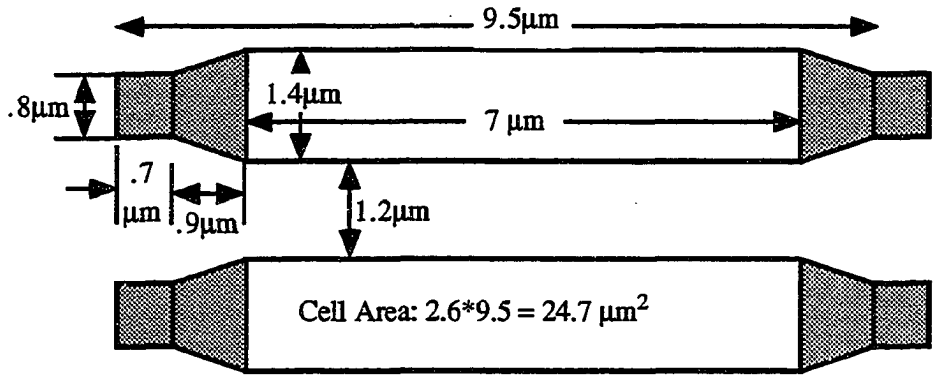


Figure 3.2 : Memory Cell used for the Design

$\Delta R = 0.005\ R_{elt} = 0.3\ \Omega$

$\therefore$ output signal available due to midline sensing in $VM = \Delta R * I_S/2 = 0.45$ mV

3.3 Feasibility Study and Modifications of the Basic Approach

The nominal output signal of a memory cell at the input to the sense amplifier is 0.4 mV. At this signal level, several factors which would have been negligible at higher signal levels become critical and need to be accounted for.

In the proposed self referencing scheme, the removal of pingpong matching array gives rise to three problems which need to be eliminated. They are as follows (a detailed analysis is given in Chapter 4) :

(1) Temperature Effects

A 10 degree increase of temperature in a memory cell is sufficient to provide an increase in cell resistance (and therefore a voltage) comparable to the signal.

(2) Bounce in Supply Voltage

To be realistic, this design allows a maximum of +/- 10 mV in the sense and gate supplies. Half of supply voltage bounce appears at the input to the preamplifier due to mid-line sensing and this can easily mask the cell output signal.

(3) Bounce in gate supply

The gate supply bounce produces approximately 0.4 mV change at the input to the preamplifier which is comparable to the signal.

The most effective solution for these problems is the use of a shared dummy sense line which reduces the effect of the above three conditions to be within safety limits as shown in Chapter 4. Since the dummy is shared among 256 sense lines in a segment, the area penalty is very low and less than 0.5%. The dummy has "0"s stored in all locations, and only provides a "0" signal reference for sensing the signal output of the accessed cell.

If only one dummy (with "0"s) is used per segment and powered up by the same drive transistors, a problem arises when the sense current is reversed to obtain the second sample. This is because the "0"s stored in the dummy now begin to act like "1"s when I_S is reversed. This can be avoided by keeping the direction of sense current (I_S) through the dummy line unchanged. That implies separate power drive transistors for the dummy and more system noise. Therefore, the best alternative is to use 2 shared sense dummy lines; one with stored "0"s for positive sense current and the other with stored "1"s for negative sense current.

With two dummies per segment, the increase of cell array size is still less than 1%. The use of 2 dummies is anyway necessary to match the RC time constants at the inputs to the preamplifier, and to match the thermal histories of dummy and accessed sense lines as explained in the next chapter.

Use of dummies introduces a new problem of large mismatch signals. This is caused by the slight variation in process parameters across a wafer which is common to any fabrication process. The sheet resistance of the magnetic double layer can vary by a maximum of 2% across a wafer. Therefore, the resistances of a sense line and a dummy can vary by 2% in a worst case scenario. This implies a maximum difference signal of about 60 mV which is much larger than the signal itself. The offset of the preamplifier which is estimated to be about 20 mV, and possible mismatch of gate transistors which results in about 15 mV maximum, too add to the above 60 mV to produce a total worst case mismatch of 100 mV.

Therefore, it is necessary to use an autozero stage to remove this difference (mismatch) voltage before the signal is turned on by powering up the word line. The straight forward approach of a single autozero stage is not good enough for this scheme because it produces too much noise as explained in Chapter 6. Therefore, a two-stage autozero, which is a high speed autozero followed by a low noise slow autozero, is used.

In previous designs (where the cell output signal was about 3 mV), autozeroing was done prior to any amplification stages. But, since the signal in this design is very small (0.4 mV compared to 3mV), the noise introduced by the autozero stage becomes critical as explained in Chapter 6. Therefore, both the signal and the mismatch voltage needs to be amplified before sending to the autozero stage. It is also necessary to locate a preamplifier at each segment to reduce glitch pickup.

There are four more critical effects, which need to be carefully analyzed in order to reduce their effect on the system reliability to negligible levels. They are listed below with the proposed solutions.

(1) Capacitive coupling between word and sense lines introduces a 2 V voltage transient at the sense supply rail when a word line is switched. This problem is solved by using a dummy word line for precharging.

(2) Inductive pickup from word lines can be as high as 2 mV in worst case conditions. This is eliminated by allowing a settling time of 10 ns.

(3) The effect of differing thermal histories of the dummy and accessed sense lines can be critical if only one dummy sense line is used. This is reduced to a manageable level with the use of 2 sense dummies which alternate during read operations.

(4) Mismatched charging time constants at the 2 inputs to the preamplifier can introduce more noise while slowing the system down. This is solved using the "balanced sensing" scheme described in the next chapter.

Above is a summary of all the problems that needed to be solved when developing the low noise front end of the sensing scheme. They are analyzed in detail in the next chapter which presents the proposed solutions.

3.4 Target Signal to Noise Ratio (SNR)

Thermal noise has a Gaussian distribution as shown in Figure 3.3 where

$$\sigma = v_{noise} = \text{sqrt}\ (4kT\Delta f R_{total}) \qquad (3.1)$$

The probability of the noise voltage, v_n being less than any voltage V is given by,

$$P(v_n<V) = 1 - 0.5 * \text{erfc}\ (V/1.41\sigma) \qquad (3.2)$$

Typically, in a memory chip, a noise induced read error rate in the range of 1 in 10^{15} is considered acceptable. Therefore, if the signal level is V_{sig},

$P(v_n<V_{sig}) > 1 - 10^{-15}$

$\therefore$ erfc $(V_{sig}/1.41\sigma) < 2 * 10^{-15}$

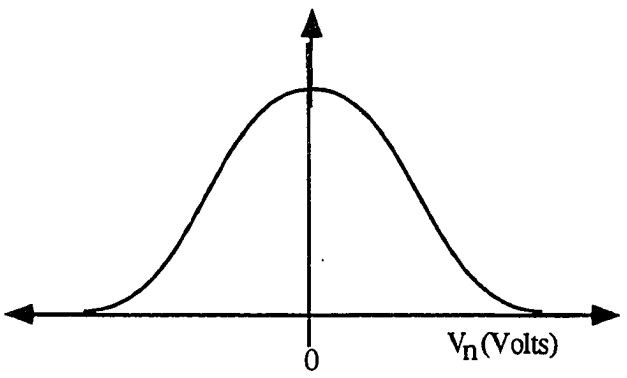


Figure 3.3 : Distribution of Thermal Noise

using the relation

$$\text{erfc}\,(x) \equiv \exp(-x^2) / (x * \text{sqrt}\,\pi) \tag{3.3}$$

for large x, the above requirement can be simplified to,

$$(\text{sqtr}(\pi/2) * V_{sig}/\sigma)^{-1} * \exp[-(V_{sig}/1.41\sigma)^2] < 2 * 10^{-15} \tag{3.4}$$

Solving the above equation, it can be seen that it necessary to have

$V_{sig}/\sigma = V_{sig}/v_{noise} \equiv 8$

to satisfy the above condition.

Therefore, it is necessary to achieve a SNR of 8 per sample. During a read operation of the proposed design, effectively 4 samples are taken. This is because two samples of the accessed cell output are taken for positive and negative sense currents, with each sample consisting of 2 measurements taken before and after the word line is turned on. The 4 samples increase the total noise by a factor of 2. Thus, it is necessary to have a SNR of 16 to account for that.

In order to keep a 2:1 safety margin, it is necessary to achieve a raw SNR of 32 for each sample.

CHAPTER 4. ANALYSIS OF CRITICAL EFFECTS

4.1 Bounce in Supply Voltage

The design allows a maximum of +/- 10 mV bounce in the sense supply voltage. A worst case bounce of 10 mV gets attenuated by a factor of 2 at the input to the sense amplifier due to midline sensing (Figure 4.1). Therefore, there is a 5 mV glitch superimposed on the signal output of the accessed line in the worst case.

When sensing with respect to a dummy, most of this 5mV is in common mode and therefore rejected by the preamplifier. The difference signal is only due to the mismatch between the accessed line and dummy. Since the mismatch due to process variations is kept under 2% for the current process,

the difference signal = 5 x 2% = 0.1 mV

Thus, the effects of supply voltage bounce is reduced to a level that wouldn't interfere with the signal.

4.2 Bounce in Gate Supply

Considering the voltage mode design in Chapter 2 with T = 25 °C, V_g = 6 V, I_S = 3mA, and V_{DD} = 3.9 V (Figure 4.2),

the gate transistor W/L = 40/0.8 = 50

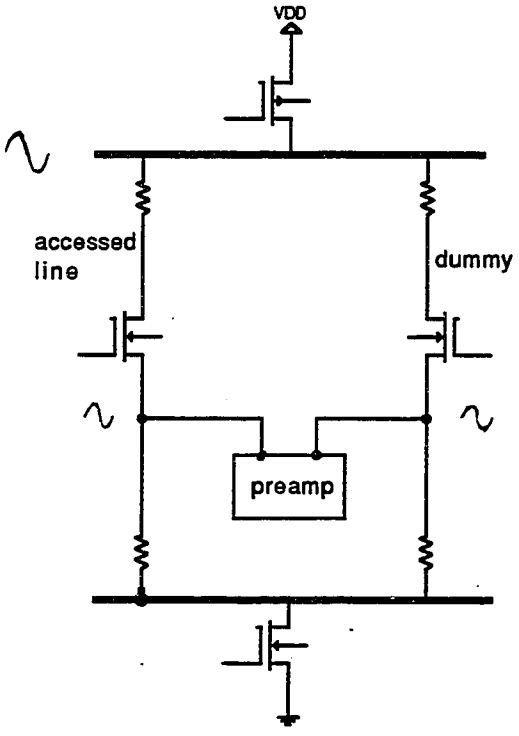


Figure 4.1 : Effect of Supply Bounce

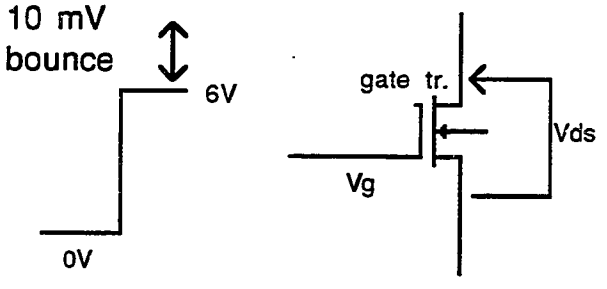


Figure 4.2 Effect of Gate Bounce

Neglecting the spreading resistance component for a first order approximation, the resistance of the gate transistor (R_g) can be found using,

$$R_g = \{K(W/L) * (V_{gs} - V_t - V_{ds}/2)\}^{-1} \quad (4.1)$$

$V_g = 6V$ => $R_g = 76.08\ \Omega$

$V_g = 6V + 10$ mV bounce => $R_g = 75.84\ \Omega$

$V_g = 6V - 10$ mV bounce => $R_g = 76.31\ \Omega$

$\therefore$ the worst case change in resistance = $\Delta R_g < 0.3\ \Omega$

Thus the gate supply voltage bounce introduces a maximum of 0.3 Ω change in drain resistance. This is a worst case scenario, because when the distributed model of gate transistor is considered, maximum ΔR_g reduces to about 0.2 Ω.

When a sense line is activated, if the drain resistance of the gate transistor changes due to gate bounce, the resulting voltage change at the input to the preamplifier is,

$\Delta R_g \times I_s/2 = 0.45$ mV

due to midline sensing.

The dummy line too is similarly affected, and about 96% of this voltage is in common mode and rejected by the preamplifier. The differential component is due to any mismatch between the gate transistors of dummy and accessed sense lines. This is about 4% in the worst case (with $\Delta V_t = 20$ mV and $\Delta K = 2.72\ \mu A/V^2$), resulting in only 18 μV which is very much less than the cell output signal of 0.4 mV.

4.3 Temperature Effects

Figure 4.3 shows the thermal environment for a 1.4 x 7 μm^2 MRAM element with 0.5 μm Silicon Dioxide insulation from the element to the substrate, and 1 μm insulation from the element to the word line conductor. The thermal conductivity of Silicon is more than 100 times that of Silicon Dioxide and therefore, the Silicon substrate can be approximated to an infinite heat sink [9]. Also, the conductor metals have thermal conductivities more than 100 times that of Silicon Dioxide and therefore the word line too can be assumed to behave as an infinite heat sink to a first order approximation.

Thus, the steady state temperature rise in MRAM elements due to the sense current can be found using,

$$\text{power dissipation} = K_{th} * \text{element area} * \Delta T * (t_{ox1}^{-1} + t_{ox2}^{-1}) \qquad (4.2)$$

where

K_{th} = Thermal Conductivity of Silicon Dioxide = 0.014 watts/cm °C.

power dissipation $= (I_s)^2 * R_{elt} = 0.54$ mW

$\therefore \Delta T = 13.12$ °C

This temperature rise increases the element resistance by 1.18 Ω which is much larger than the change in element resistance when the word current is applied.

By using a dummy, it is possible to make the voltage change resulting from increase in element resistance due to heating effects, be in common mode at the input to the preamplifier.

In order to achieve this, both the dummy and the accessed sense line should have similar thermal histories. If only one shared dummy is used, it is possible for the dummy to

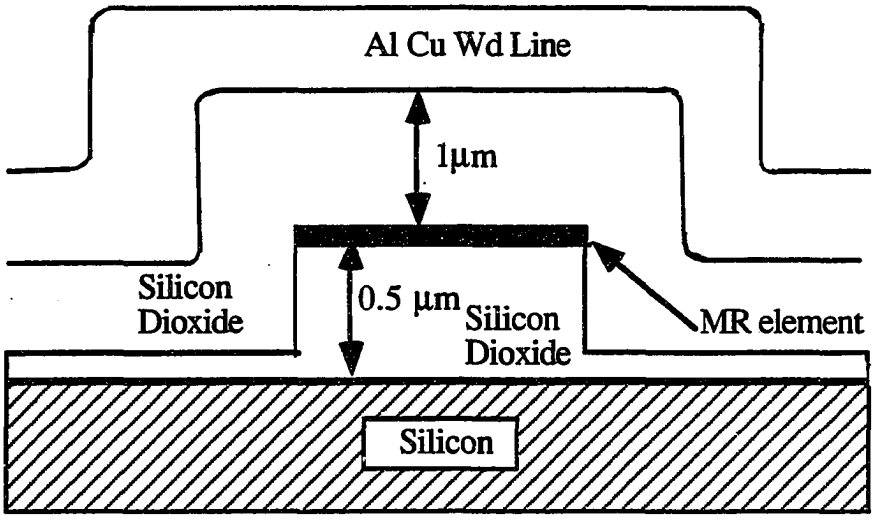


Figure 4.3 : Memory bit Cross Section

be at a higher temperature than the accessed sense line since dummy is always activated during a read operation. Since there are two dummies used in this design with each dummy active only for a half of a read cycle, both dummies get sufficient time (half a cycle) to cool down before being activated again. Simulations have shown that the mismatch due to different thermal histories are minimal under these conditions [9].

4.4 Inductive Pickup from Word Lines

Figure 4.4 shows the layout of word lines and sense lines in a cell array. It can be seen that a spike can be generated in the sense rails due to inductive pickup when the word current is switched on. This can be estimated as follows.

The field due to word current (I_w) is given by,

$$H = 0.2\, I_w / r \quad Oe \tag{4.3}$$

where 1 Oe = 1 line / cm^2

Integrating H between 5 μm and 200 μm,

flux per unit length of sense rail = $0.74\, I_w$ lines/cm

$\therefore$ total flux in the sense loop is given by,

$$\phi = 0.74\, I_w * 400 * 10^{-4} = 0.03\, I_w$$

Converting to mks units and substituting for I_w which is 30 mA in this design,

$\phi = 9 \times 10^{-12}$

If the word current is assumed to turn on in 10 ns, the induced spike is given by

$$v_{in} = d\phi/dt = 0.9 \text{ mV} \tag{4.4}$$

Therefore, the worst case glitch due to inductive pickup is 0.9 mV, and by allowing about 10 ns for it to die down, this effect can be eliminated.

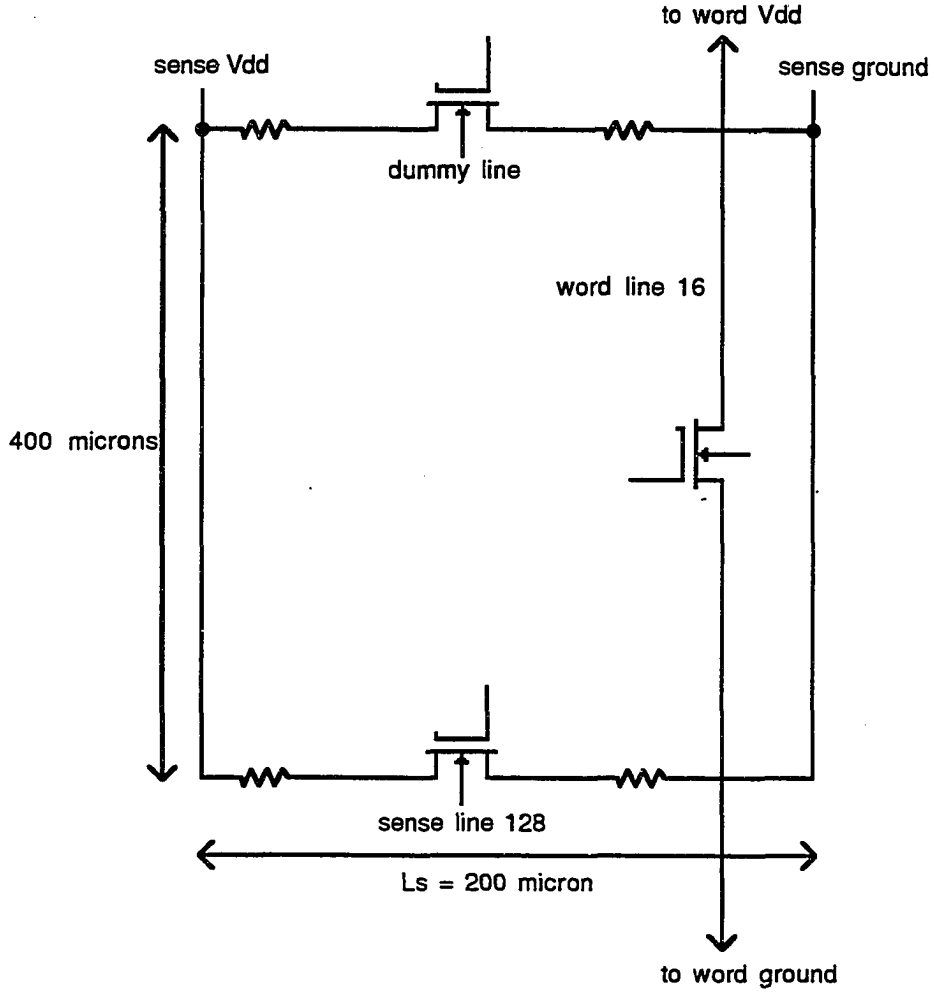


Figure 4.4 : Word and Sense Line Layout in Cell Array

4.5 Capacitive Coupling between Word and Sense Lines

The capacitive coupling from word rail to a sense rail at each memory element is given by,

$$C_{ws} = \varepsilon_{SiO2} * \text{Element area / oxide thickness} \quad (4.5)$$

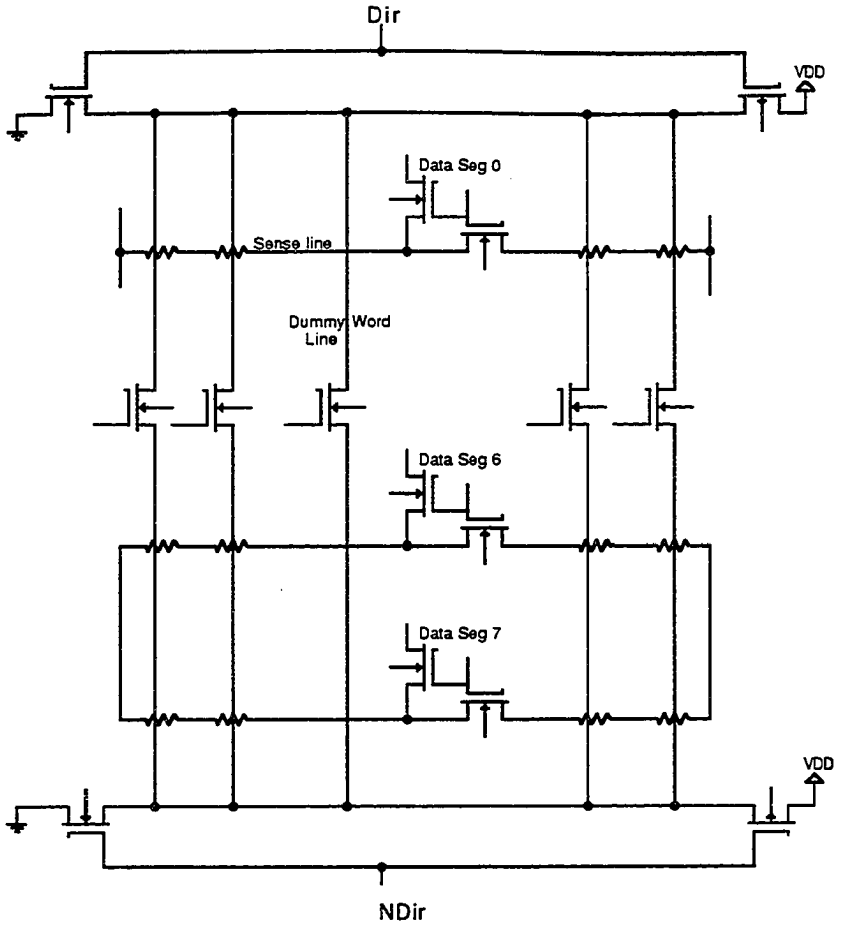
For the current process, this is approximately 0.4 FF per bit (Figure 4.5). Since there are 4000 memory elements in a segment, the total coupling capacitance can be lumped as 1 pF at each sense power rail as shown in the approximate model of Figure 4.6.

When a word line is switched on, approximately 2V of voltage transient occurs at the word rail [3]. Assuming that this occurs in 10 ns, the generated current transient at sense rails is found using,

$$i_{tran} = C\, dv/dt \quad (4.6)$$

This current transient of 0.2 mA produces voltage transients of 20 mV at the positive sense rail and 14 mV at the sense ground rail. This glitch occurs after autozeroing is done and a considerable amount of time has to elapse before it dies down.

This effect is minimized using a dummy word line (with no cells underneath) which is switched on at the beginning of a read cycle to precharge. Once autozero is completed, the word line which accesses the bit is switched on. Now, the transient at word rail is only due to the mismatch between the dummy word line and the accessed word line which is typically less than 5%. Therefore, the voltage transient at sense rails reduce to 1mV at the positive rail and 0.7 mV at the ground rail which will die down in approximately 10 ns time.



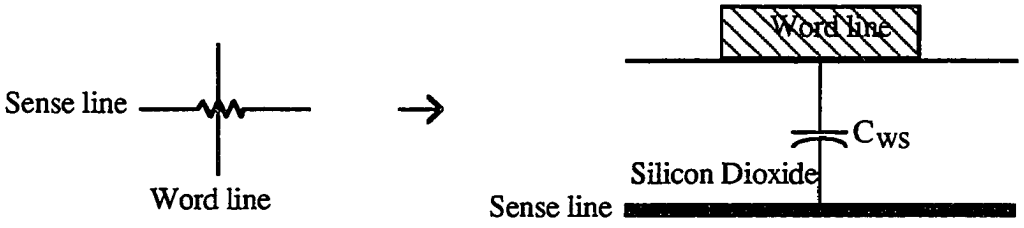


Figure 4.5 : Coupling Capacitances between Word and Sense Lines

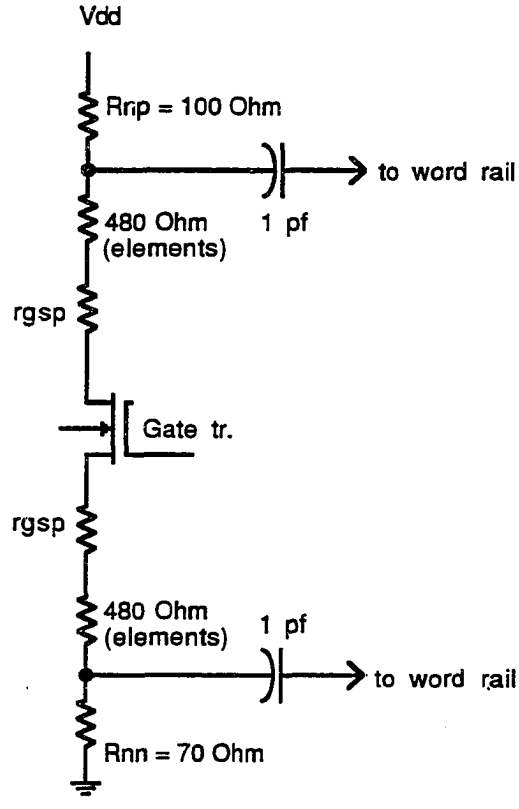


Figure 4.6 : Lumped model of Coupling Capacitances

4.6 Balanced Sensing to Match RC Time Constants

The original scheme was to connect the 256 sense lines in a segment to one input of the preamplifier and connect the 2 dummy lines to the other input. This scheme (Figure 4.7) introduces a substantial amount of noise due to the non-uniform capacitive loading at the inputs to the preamplifier.

As shown in Figure 4.8, the charging time constants at the 2 inputs to the preamplifier differs by a factor of 128. Therefore, the glitches which are in common mode (and are expected to cancel each other), themselves generate a considerable difference signal across the preamplifier inputs. Also, it takes a long time to reduce the effect of different charging time constants.

The new balanced sensing scheme eliminates the above problem by dividing the number of storage sense lines in a segment equally between the 2 input transistors of the preamplifier (Figure 4.9). The 2 dummy lines have 2 mux transistors each enabling them to be switched between the 2 inputs of the preamplifier. If the group of sense lines containing the accessed sense line is connected to one input of the differential pair, the active dummy is switched on to the other input together with the other half of sense lines in the segment. The inactive dummy is switched on to the input where the accessed sense line connects and thus, the charging time constants at each input of the differential pair are made equal.

Therefore, the problem due to different charging times is eliminated and there will be no differential component left from common mode signals due to mismatched charging times. Thus, the balanced sensing results in a highly improved SNR performance compared to the scheme in Figure 4.7.

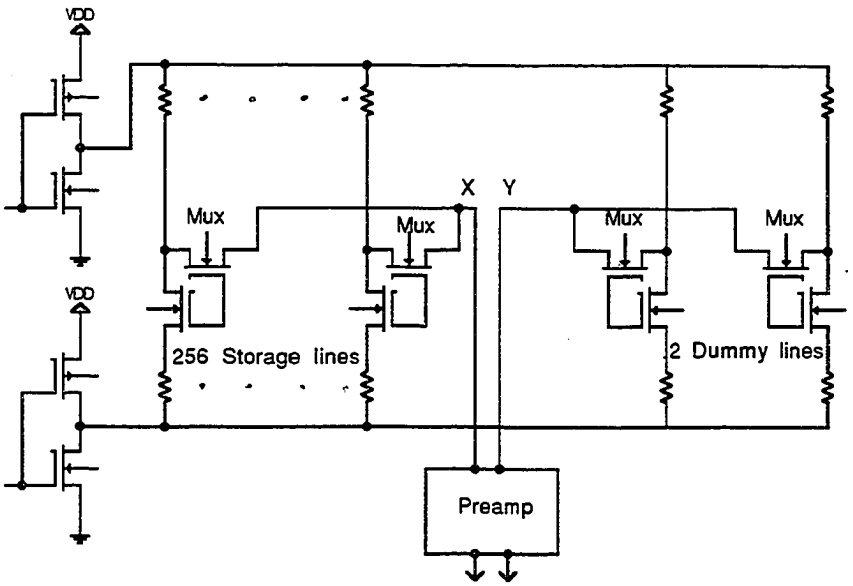


Figure 4.7 : Original Scheme with Imbalanced RC Time Constants

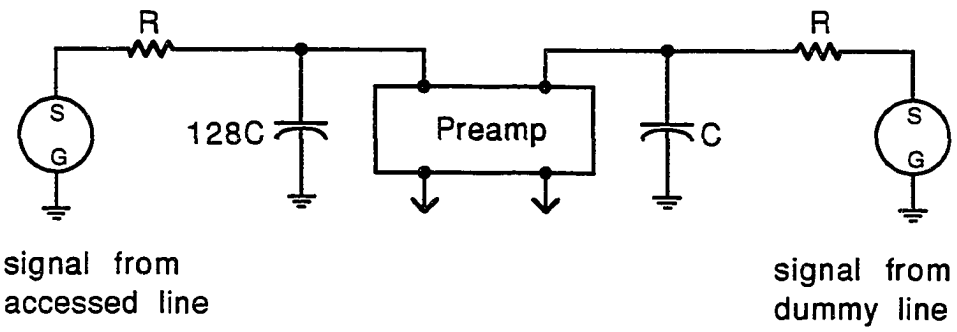


Figure 4.8 : RC Model for Figure 4.7

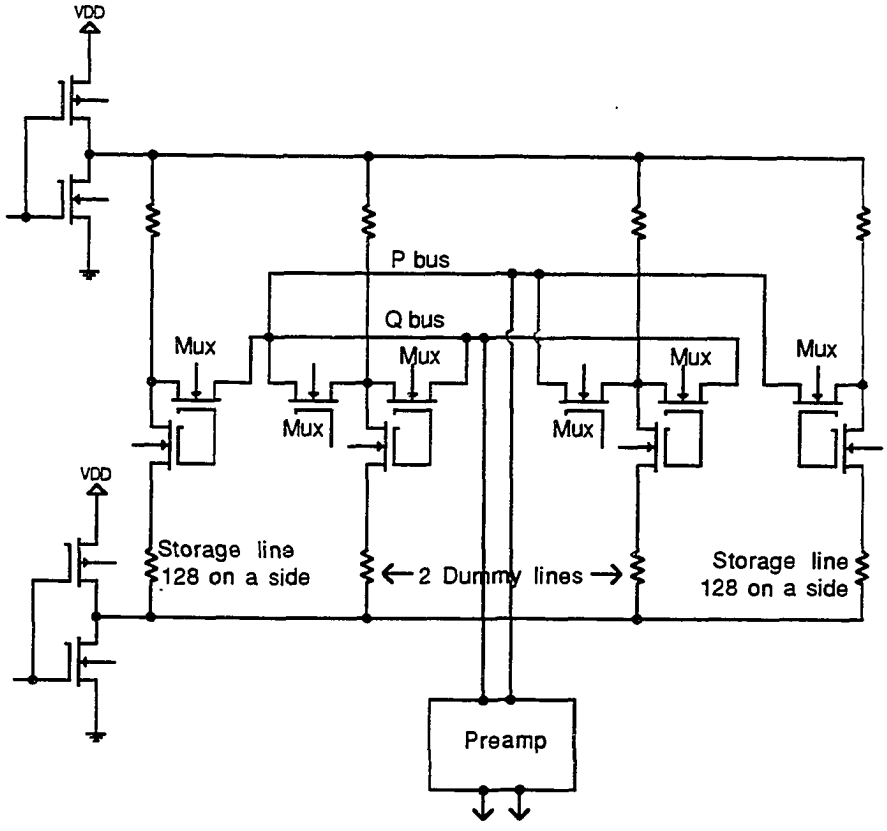


Figure 4.9 : New Balanced Sensing Scheme

CHAPTER 5. PROPOSED SENSING SCHEME

5.1 Block Diagram

Figure 5.1 presents the block diagram of the proposed sensing scheme, which senses the very small output signal of a memory cell and amplifies it to full logic levels.

Sense lines are grouped into segments (1 segment = 256 sense lines) each with its own preamplifier in order to minimize noise effects. The sensing is in voltage mode with mid-line sensing. A sense line contains 16 memory cells each with 60Ω resistance.

The nominal signal at the center of the line is 0.45 mV with a 100 mV (maximum) of mismatch. There are 2 shared dummy sense lines per segment for auto-zero purposes. And the array is "balanced" for better signal to noise performance.

The output signal of a memory cell is sensed with respect to that of a dummy cell. This difference signal plus the mismatch voltage is amplified by the preamplifier which is a low noise differential amplifier with a low gain of 10. Each segment has its own preamplifier.

The amplified output of the preamplifier (4mV signal + 1 V mismatch), is then routed to subsequent stages of the sense amplifier which are shared among all segments. There the fast autozero circuit removes most of the mismatch voltage generated by the process parameter variations across the die.

The next stage, which is a differential amplifier with a gain of 10 (output is 40 mV), isolates the fast autozero circuit from the slow autozero circuit. Next, the slow autozero stage removes any remaining mismatch and limits the noise effects of the fast autozero.

Then the differential signal is converted to a single ended signal in diffamp 3 which has a gain of 5. At this point, the signal is amplified to 200 mV. The bandwidth of all stages till now is quite high, and tend to pass through a large portion of the noise generated by the elements. Therefore, a bandwidth limiter is used to filter out and reduce this noise.

Then the signal is fed to a sample and hold circuit which holds the first sample (obtained with positive sense current), and compares with the second sample (obtained with negative sense current), to produce a logic level output [11].

The front end of this sensing scheme, including the fast autozero circuit is explained in detail in the next chapter. The other stages are described in reference [11].

5.2 Timing

Figure 5.2 shows the timing for the proposed sensing scheme.

t1 : Address decoding = 30 ns

t2 : Switching and settling time for the MR element array = 20 ns

At the beginning of t2, gate, mux and sense drive transistors are switched on. The dummy word line too switches on at this time to precharge.

t3 : Fast autozero time = 60 ns

The fast autozero transistors which have been on since the beginning of the cycle switches off at the end of t3. Slow autozero transistors switch on at the beginning of t3.

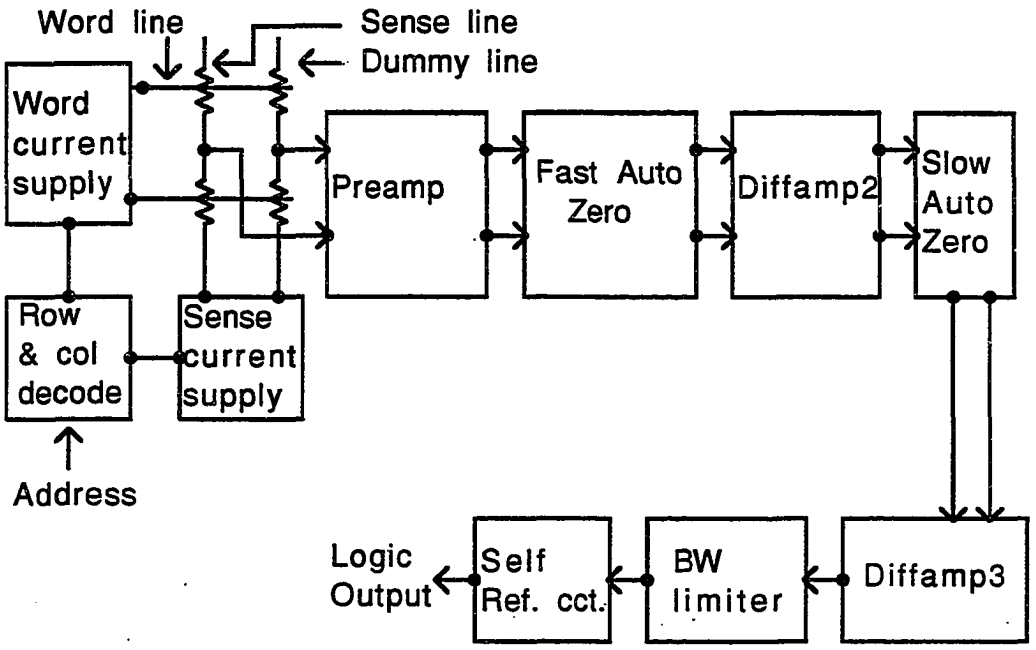


Figure 5.1 : Block Diagram of the Proposed Sensing Scheme

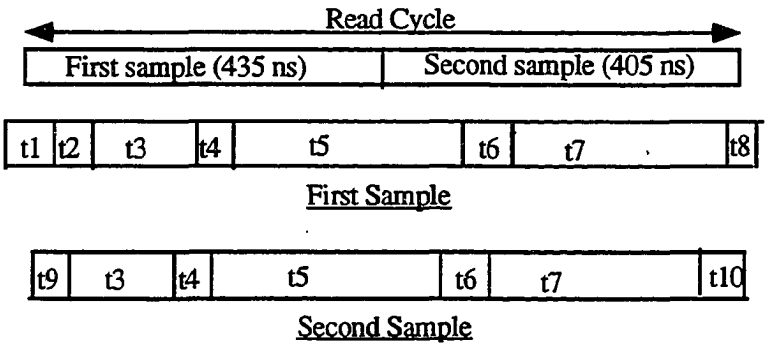


Figure 5.2 : Timing for a Read Cycle

t4	:	Diffamp 2 offset removal time	= 20 ns
t5	:	Slow autozero time	=150 ns
t6a	:	Wait time before turning on the word current	= 10 ns
t6b	:	Wait time for settling after turning on the word current	= 10 ns
t7	:	Delay of BW limiter and sampling time	= 125ns
t8	:	Wait time before reversing the sense current	= 10 ns
		The slow autozero transistors and the sense drive transistors switch off at the end of t8. The first sample is stored in the sample and hold stage at the end of t8.	
t9	:	Switching and settling time after reversing the sense current	= 20 ns
t10	:	Latching time	= 10 ns
		Logic level output is latched at this point.	

A detailed explanation of the timing diagrams is given in reference [11].

CHAPTER 6. SENSE DRIVER CIRCUITS

6.1 Circuit Description

This circuit is designed to meet two main requirements.

(1) Thermal Stability

It is necessary to maintain a constant sense current for read operations, at all temperatures within the operating range (0 °C to 75 °C). This is achieved by using a temperature compensated, regulated power supply. The supply voltage (V_{DD}) is varied linearly from 3.8 V to 4.3 V over the operating temperature range.

(2) Constant input bias to the Preamplifier

The bias voltage at the input to the MUX transistor (Vsen) should be maintained at approximately 2V for both polarities of read sense current and over the operating temperature range (Figure 6.1). This is necessary since Vsen becomes the common mode input signal to the differential preamplifier. (Any large drifts in this voltage can drive the preamplifier out of its linear region causing errors.)

The sense current supply (Figure 6.1) consists of 2 push-pull driver pairs (M2 and M5, M3 and M6). The gate inputs Vcon1 and Vcon2 control the direction of sense current.

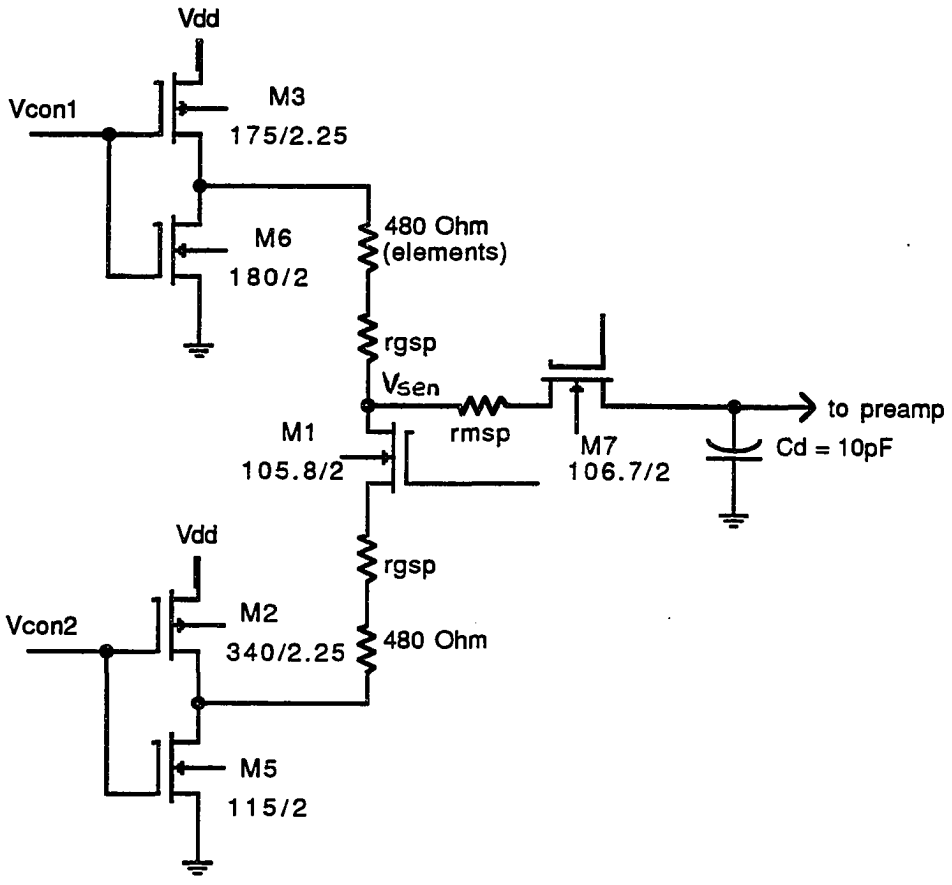


Figure 6.1 : Sense Current Driver Circuits

(Vcon1 = INV(Vcon2)) When Vcon1 is high, Vcon2 goes low, and only M2 and M6 are active. Then the direction of sense current is negative.

Since the 16 MR elements on a sense line take up a total of 2.88 V across them, the head room left for the transistors are small. And the regulated supply of about 4.3 V is not sufficient to keep the drop across gate transistors reasonably low. Therefore a sense gate supply of 6 V is generated on chip for the gate signals of mux and gate transistors.

By sizing the driver transistors as shown in Figure 6.1, it was possible to maintain the bias voltage at Vsen within reasonable limits over the temperature range and for both polarities of sense current. The W/L ratios of the buried MUX and GATE transistors were limited to 106.75/2 and 105.8/2 respectively to achieve maximum cell density [3].

The drivers supply a total of 5.6 mA (2.8 mA per sense line) during a read operation and 3.2 mA during write operation. The Vds values of the active transistors adjust automatically to accommodate this.

The source and drain spreading resistances of the central gate transistor were estimated manually (using the model explained in Chapter 2) and lumped at either side of the gate transistor for simulations. (The VTI extractor does not extract spreading resistance values from layouts.) The control signals Vcon1 and Vcon2 are derived from the temperature compensated power supply to keep the drift of Vsen to a minimum.

Results obtained from simulations carried out over the full temperature range is given in Table 6.1.

6.2 Noise Estimations

A noise analysis was performed to find the noise generated at the input to the preamplifier (including preamplifier noise) in the worst case which is at 75 °C with the

Table 6.1 : Simulation Results of the Sense Driver Circuits

Isense polarity	Temp. (C)	Vdd (Volts)	Vcon1 (Volts)	Vcon2 (Volts)	Vsen (Volts)
+	0	3.8	0.0	3.8	1.89
+	25	3.97	0.0	3.97	1.97
+	75	4.3	0.0	4.3	2.14
-	0	3.8	3.8	0.0	1.72
-	25	3.98	3.98	0.0	1.8
-	75	4.3	4.3	0.0	1.86

sense current polarity set to positive. The equivalent noise resistances are shown in Figure 6.2.

signal level = 0.417 mV

the system BW till the input to the preamplifier = 28 MHz (calculated in Section 6.4)

$\therefore$ the noise before bandlimiting = 27.8 μV

The bandwidth limiter circuit sets the system bandwidth to 5 MHz in order to limit thermal noise [11].

the noise after bandlimiting = 11.75 μV

$\therefore$ the Signal to Noise ratio = 35.4

Thus the SNR needed to limit the noise induced errors to less than 1 in 10^{15} is achieved.

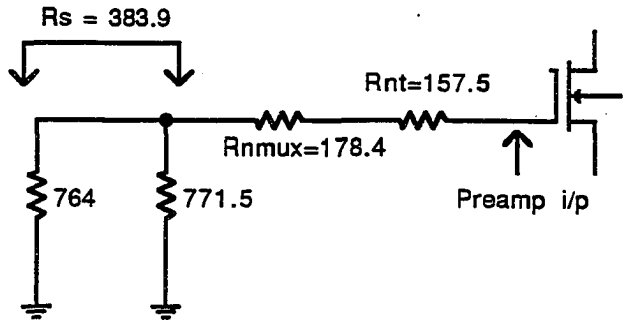


Figure 6.2 : Equivalent Noise Resistances

6.3 Drain Capacitance of the Mux Transistor

Since the mux transistor is operating in Ohmic region, the total capacitance at its drain is given by,

$$C_{dmux} = C_{db} + C_{gd} + C_p \qquad (6.1)$$

where

C_{db} = CJ * Drain Area = Junction capacitance at drain

$C_{gd} = C_g/2$ = Gate to drain capacitance in Ohmic operation

C_p = CJSW(N) * Peripheral length = Peripheral capacitance of drain

Since CJ = 238 x 10^{-6} F/m^2, C_g = 2 FF/μm^2 and CJSW(N) = 4.43 x 10^{-10} F/m for the process used,

C_{dmux} = 71.31 FF $\cong$ 72 FF

6.4 Estimation of RC Time Constant and Bandwidth

The small signal equivalent RC circuit till the preamplifier input is shown in Figure 6.3. Since each input of the preamplifier is fed by 130 Mux transistor lines, the total drain capacitance at each input to the preamplifier is represented by C_{dt} where

$C_{dt} = C_{dmux} \times 130 = 9.36$ pF

Since the preamplifier's input transistors are in saturation,

$C_{gs} \cong (2/3) * C_g = 0.63$ pF

$\therefore C_{dt} + C_{gs} = 10$ pF

The time constant of this circuit can be approximated by

$$\tau = (R_s + R_{mux})(C_{dt} + C_{gs}) \qquad (6.2)$$

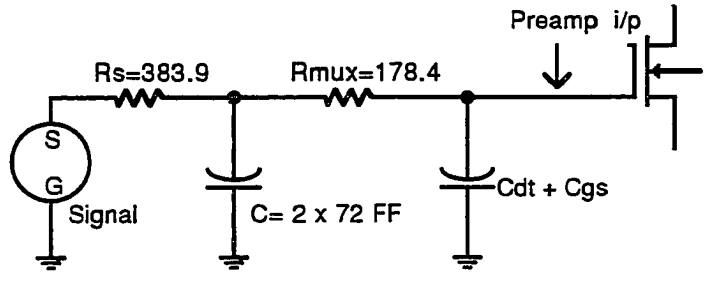


Figure 6.3 : Equivalent RC Network

to give $\tau = 5.6$ ns.

The system bandwidth is given by,

$$BW = 1/2\pi RC \tag{6.3}$$

to be 28 MHz. This high bandwidth is limited by the bandwidth limiter stage to reduce noise.

A transient analysis was performed to estimate the settling time of Vsen. The resulting waveform is shown in Appendix. Time constant for this circuit was found to be about 6 ns as estimated. Since preamplifier and Fast Auto Zero circuits are of very high bandwidth, about 10 time constants of of settling time is sufficient for the fast autozero to complete.

CHAPTER 7. PREAMPLIFIER

7.1 Circuit Description

Two possible approaches were considered when designing the preamplifier. One approach was to use a self biased inverting amplifier (Figure 7.1). There B1 functions as the bias transistor which ensures that the inverter is always biased in the linear region, by momentarily shorting the input to the output (Vin = Vout = $V_{DD}/2$). This is done after the mux transistor switches on, and C1 charges up to the difference voltage between the output of the sense circuit and $V_{DD}/2$. Then B1 is turned off and the word line is switched on.

Though this design is conceptually simple, several problems exist. One problem is the high gain of this stage which is a function of the process parameters. (A gain much higher than 10 would saturate the following amplifier stages.) There also exists a problem of feedthrough. When B1 switches off after setting the bias, some charge is fed through gate-drain capacitance of B1 to the gates of M1 and M2 creating an offset. This can be reduced by connecting a properly sized transistor with its drain and source shorted to point X, and switched by the complement of CONB1. It may also be necessary to remove the mismatch before this amplifier in order to keep it in the linear region.

Therefore, the second approach of differential pair was selected for this design (Figure 7.2).

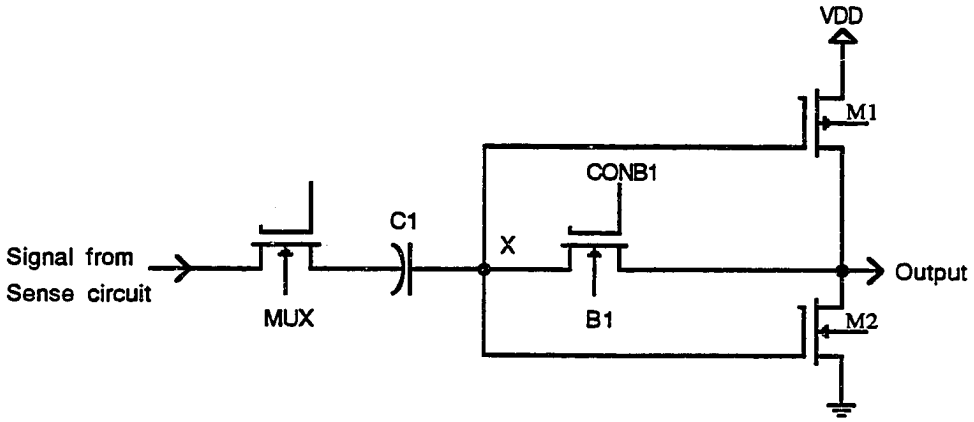


Figure 7.1 : Self Biased Inverter

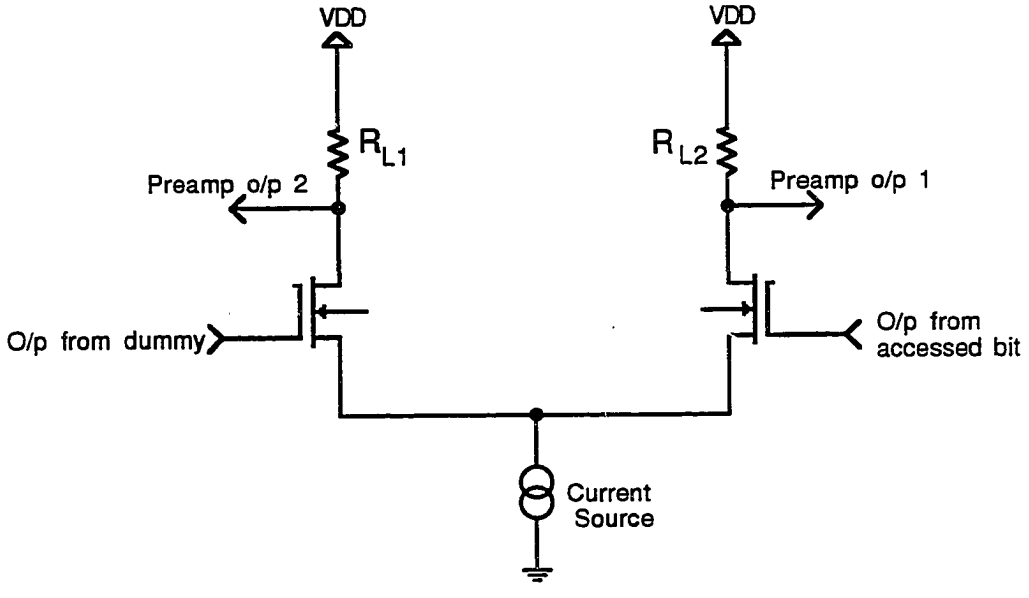


Figure 7.2 : Differential Pair

In order to maintain a SNR of 32 at the inputs to the preamplifer, the preamplifier noise resistance referred to the gates of the input pair should be approximately 125 Ω or less. Since the input transistor pair operate in saturation, each has an equivalent noise resistance of

$$R_n = 2 / 3g_m \tag{7.1}$$

at the gate. The current source noise is in common mode and therefore gets cancelled off. The equivalent noise resistance of the load resister R_L referred to the gate is given by,

$$R_{nL} = R_L / G^2 \tag{7.2}$$

where G is the gain of the preamplifier.

Therefore, the total equivalent noise resistance of the preamplifer is given by,

$$R_{nt} = (2/3g_m) + (R_L / G^2) \cong 2/3g_m \tag{7.3}$$

since the gain is quite large.

In order for the amplifier equivalent noise resistance to be 125 Ω, the input transistors need a g_m of 0.0053 or higher. Since the amplifier gain is given by

$$G = g_m R_L \tag{7.4}$$

the estimated load resistance is 1.88 kΩ.

It is not possible to use a saturated load since a transistor in saturation has a very high resistance in the region of 50 -100 kΩ. Even transistors biased in linear region is not a good choice because they are difficult to match and are only linear over a certain range. They require a complex bias generator circuit and offer no real advantage other than a small area saving.

Therefore, permalloy resistors were selected for load resistors. These can be matched very well when placed close to each other and has an adequate sheet resistance of 10 Ω/sq. Since the required load resistance is only about 2kΩ, this implies permalloy resistors with W/L = 200, which isn't all that big. Therefore, permalloy resistors were selected for this design. The current source is implemented using a single n-channel transistor biased with an accurate reference voltage.

7.2 Transistor Sizing

The average input bias to the preamplifier ≅ 2.01 V

Since $g_m = K (W/L) (V_{gs} - V_t)$ and gm needs to be larger than 0.00533, a W/L ratio of 183.5 is selected for the input transistor pair.

$\therefore I_{ds} = 0.95$ mA

Also, there is a sufficient voltage drop across the input transistors to keep them in saturation.

For the current source transistor,

$I_d = 1.9$ mA

Selecting $V_{gs} = 1.3$ V,

W/L = 323.5

Simulations have shown that Flicker noise component is negligible at the operating frequency of 5 MHz [1]. Anyway, Flicker noise effects can be minimized by increasing the area of input transistors and reducing the bias current. Also, the use of minimum length transistors introduces the problem of channel length modulation. Therefore,the input transistor pair is made large with W/L = 293.6/1.6.

The current source transistor was sized to have W/L = 388.2/1.2 in order to reduce channel length modulation effects. The bias voltage of 1.3 V is generated using a conventional voltage divider.

After doing simulations which take second order effects into account, it was found that R_L needs to be increased to 2.2 kΩ to achieve the specified gain of 10.

7.3 Bandwidth Estimations

The output impedance of the preamplifier is given by,

$$R_{out} = R_L // r_o \tag{7.5}$$

where r_o is the output resistance of the input transistor. Since it is in saturation,

$r_o = 1/ I_d * \lambda \cong 50\ k\Omega$

$\therefore R_{out} = R_L = 2.2\ k\Omega$

The drain capacitance at the output is given by ,

$$C_d = C_{db} + C_{gd} + C_p$$

where

C_{db} = junction capacitance at drain

C_{gd} = gate drain overlap capacitance (since transistor is in saturation)

C_p = peripheral capacitance of drain

$\therefore C_d = 0.44$ FF

Therefore, the no load time constant $\tau = R_L * C_d = 0.96$ ps and the estimated bandwidth is 165 MHz.

7.4 Simulation Results

The use of permalloy resistors helps to hold the gain approximately steady over the temperature range. As the temperature increases, the g_m of the input pair reduces, but the load resistance increases. Since $G = g_m R_L$, this helps to reduce the change in G with temperature.

Extensive simulations showed that the use of a temperature compensated power supply is not essential to maintain stability. Therefore a regulated supply of 4.3 V is used. The slight shift in the output voltages with temperature is in common mode and eliminated in the following stages.

Simulations carried out for a common mode input range of 1.7 V to 2.15 V, a 50 mV variation in V_t, and full temperature range showed the differential gain to be stable at 10 with a linear region of approximately 0.4 V, which is sufficient for the expected input signal of 0.4 mV plus the 0.1 V mismatch (Appendix). The amplifier bandwidth was found to be about 150 MHz (Appendix).

CHAPTER 8. FAST AUTOZERO CIRCUIT

8.1 Circuit Description

This stage is necessary to remove the offset voltage due to process parameter variations and the offset in the preamplifier.

In previous designs, the cell output signal is directly sent to an auto-zero stage (Figure 8.1) to remove mismatch before any amplification is done. With a nominal signal level of 0.4 mV, this is not very practical because of the following reasons.

1. Insertion of auto-zero circuitry before the preamplifier increases the noise level since the auto-zero transistors themselves generate noise.
2. Auto-zero capacitors and wiring are prone to glitch pickup. This effect is reduced if the signal is stronger.

Therefore, in this design, the memory cell output is immediately amplified at the segment itself to keep the noise down.

The delay in auto-zero time is reduced by using a two stage auto-zero with

1. a fast auto-zero stage after the preamplifier to quickly reduce the 1 V mismatch to less than 4 mV.
2. a slow auto-zero to further reduce that mismatch to about 0.1 mV while keeping the noise introduced by the auto-zero transistors to a minimum.

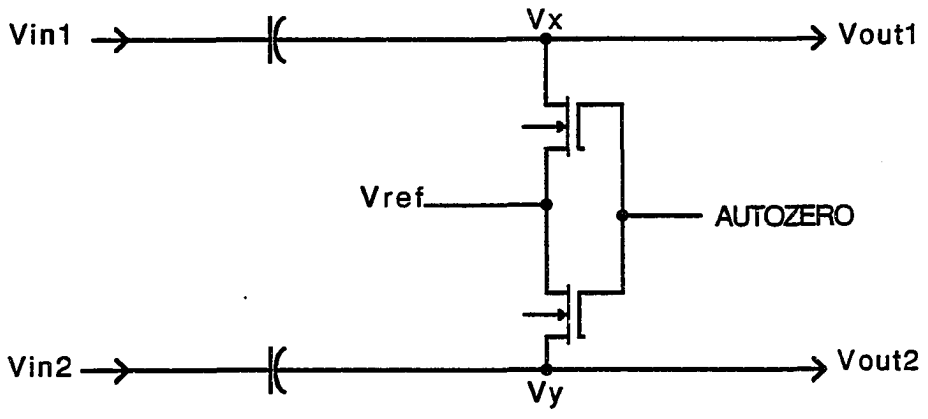


Figure 8.1 : Autozero Circuit

8.2 Device Selection and Sizing

The preamplifier and fast autozero circuits are shown in Figure 8.2. The fast autozero circuit is designed to achieve a small RC time constant. The resistance of the autozero transistor, R_a is given by,

$1/R_a = K(W/L)\,[V_{gs} - V_t - V_{ds}]$

A minimum size transistor with W/L = 5/2.5 is selected to obtain a resistance of 2 kΩ.

$\therefore V_{ref} = 2.3$ V

(V_g is set to be 6 V.)

The autozero capacitor is constructed by connecting the two floating capacitances of metal 2 to metal 1 and metal 1 to poly in parallel (Figure 8.3). Therefore, the useful capacitance is given by,

$C_a = 1 \times 10^{-4}$ pF/μm^2

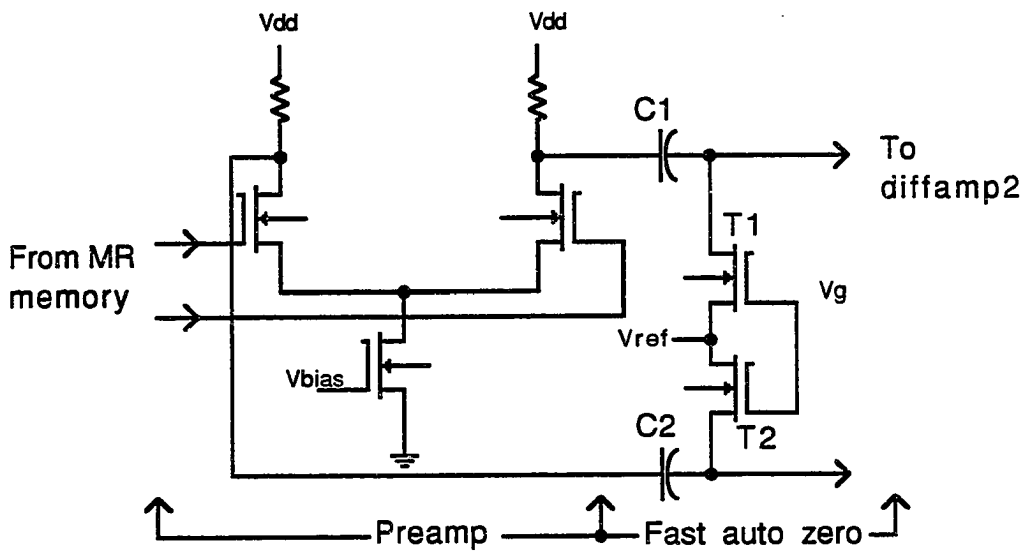


Figure 8.2 : Preamplifier and Fast Autozero Circuits

This scheme has an inherent parasitic capacitance C_p from poly to substrate which is given by,

$C_p = 6.5 \times 10^{-5}$ pF/μm^2

The autozero capacitance C_a is set to 0.3 pF. Therefore, this implies a capacitor area of 3000 μm^2.

8.3 Circuit Analysis

The small signal equivalent circuit of the autozero stage is shown in Figure 8.4, where

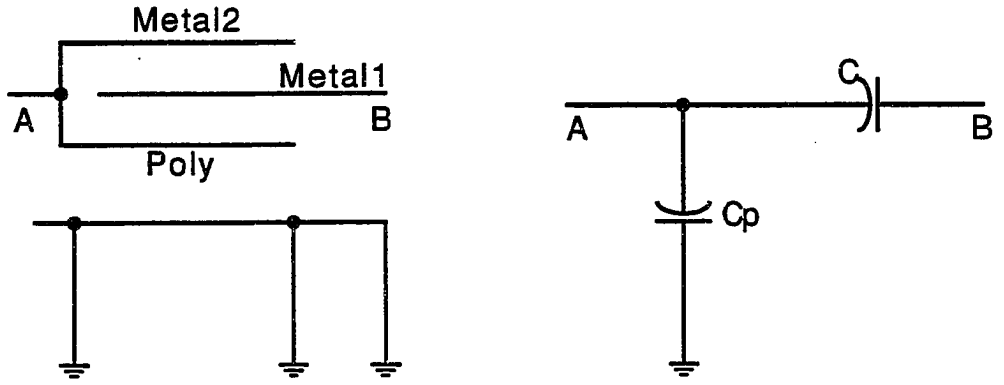


Figure 8.3 : Autozero Capacitor

R_o = output resistance of the preamplifier = 2.2 kΩ

C_d = drain capacitance at the preamplifier output = 0.44 FF

C_a = autozero capacitance = 0.3 pF

C_p = parasitic component of autozero capacitor = 0.195 pF

R_a = resistance of the autozero transistor = 2 kΩ

C_{da} = drain capacitance of the autozero transistor ≅ 0.008 pF

C_g = gate capacitance of the diffamp 2 input transistor ≅ 0.075 pF [11]

The time constant of the autozero stage can be approximated by,

$$\tau = C_a (R_o + R_a) \cong 1.3 \text{ ns} \qquad (8.1)$$

The noise generated by the resistors R_o and R_a in the equivalent circuit of Figure 8.4 is estimated as follows;

$$\text{noise voltage due to Ra} = \text{sqrt}\,(4kT\Delta f * Ra) \qquad (8.2)$$

For a first order low pass filter,

Δf = effective noise BW = 1.57 x 3 dB BW

and the 3dB BW $\equiv 1/(2\pi RaCa)$

$\therefore$ noise voltage due to Ra $= \text{sqrt}\,(4kTRa * 1.57/(2\pi RaCa))$

$= \text{sqrt}\,(4kT * 1.57/(2\pi Ca)) \equiv 0.12$ mV

Similarly,

noise voltage due to Ro $= \text{sqrt}\,(4kT * 1.57/(2\pi Ca)) * (Ra / (Ra + Ro))$

$\equiv 0.06$ mV

The charge stored in the autozero capacitors due to element noise can be estimated as follows;

system BW (till fast autozero) = 28 MHz

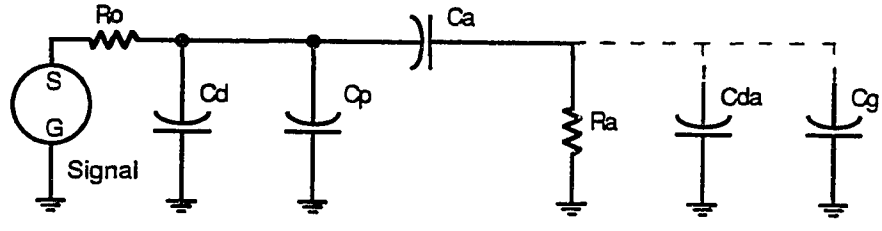


Figure 8.4 : Small signal equivalent circuit

$\therefore$ equivalent noise bandwidth (ENBW) = 44 MHz

Since the element noise after limiting the bandwidth to 5 MHz was found to be 11.75 μV (see Chapter 6.2), the noise charge can be found using,

noise charge = 0.707 * Band limited noise * Preamp gain * sqrt (ENBW/5 MHz)

Thus, the noise charge due to the memory elements amounts to 0.252 mV.

$\therefore$ total noise voltage = 0.3 mV

The signal attenuation due to fast autozero can be estimated using

$G = Ca / (Ca + Cda + Cg) \cong 0.78$

Therefore, the signal is attenuated to 78 % of that at the input to the autozero stage.

It is necessary to reduce offset at the input to the preamplifier to 10% of the noise charge on both capacitors.

$\therefore$ offset = 0.3 * sqrt(2) / 10 = 42.4 μV

In order to reduce the offset to 42.4 μV, assuming a 10% error in the system time constants, the wait time should be at least 11 time constants ($\cong$ 60 ns).

CHAPTER 9. CONCLUSIONS

Eventhough the MRAM technology was originally developed for space and military applications, it has been found to be well suited for commercial applications as well.

The sensing technique presented in this thesis is designed for such an application, in high density memories. The technique uses a new mode of sensing ("voltage mode") which is superior in performance to the existing "current mode" sensing. Also, voltage mode sensing is less affected by scaling of dimensions and voltages.

The proposed sensing scheme achieves high density by sensing very small signal outputs of small memory cells, and eliminating the usual "ping pong" matching array. This scheme, which was developed for magneto resistive materials with a MR coefficient of 2.5%, senses a nominal signal of 0.4 mV in a 800 ns read cycle.

MRAM technology, which is still in the research stages has been developing very rapidly during the past few years. The discovery of Giant Magneto Resistance (GMR), which improves the MR coefficient by more than 100%, has been a giant leap forward in this development process. GMR materials developed so far have achieved a MR coefficient in the range of 6.5% - 8% with a sheet resistance of 25 Ω/sq. If the proposed sensing scheme is used on GMR cells, it is possible to improve the density by a factor of 2 while improving the signal level by a factor of 3. This implies a possible speed up of 4 to 8 times with access time in the range of 100 - 250 ns.

Therefore, with the use of GMR materials, MRAMs have the potential to surpass the performance levels of DRAMs and other popular memory technologies, and probably become a contender to a large portion of the computer memory market.

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APPENDIX . SIMULATION RESULTS

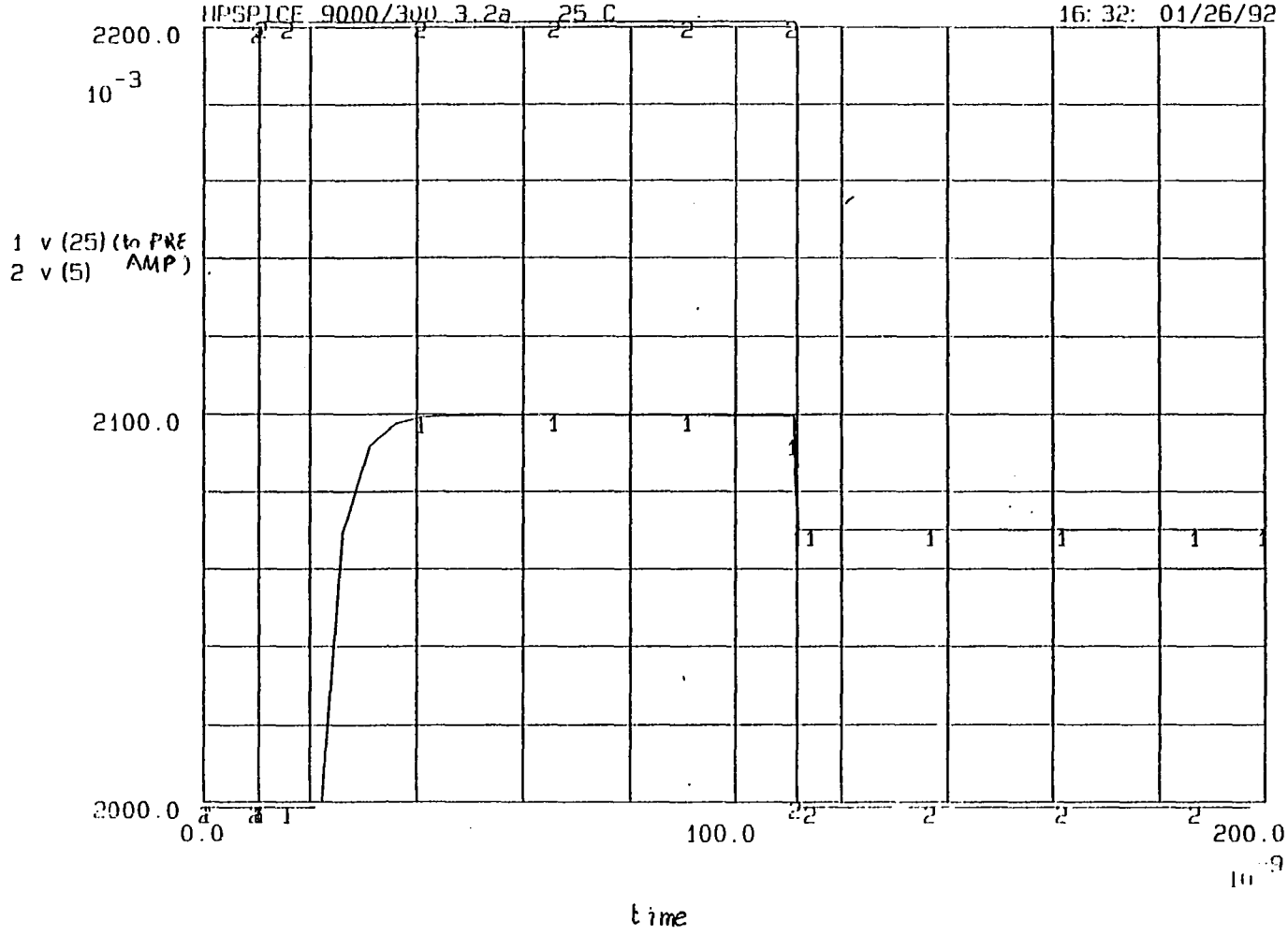

Figure A.1 Transient Response of the Sense Lines

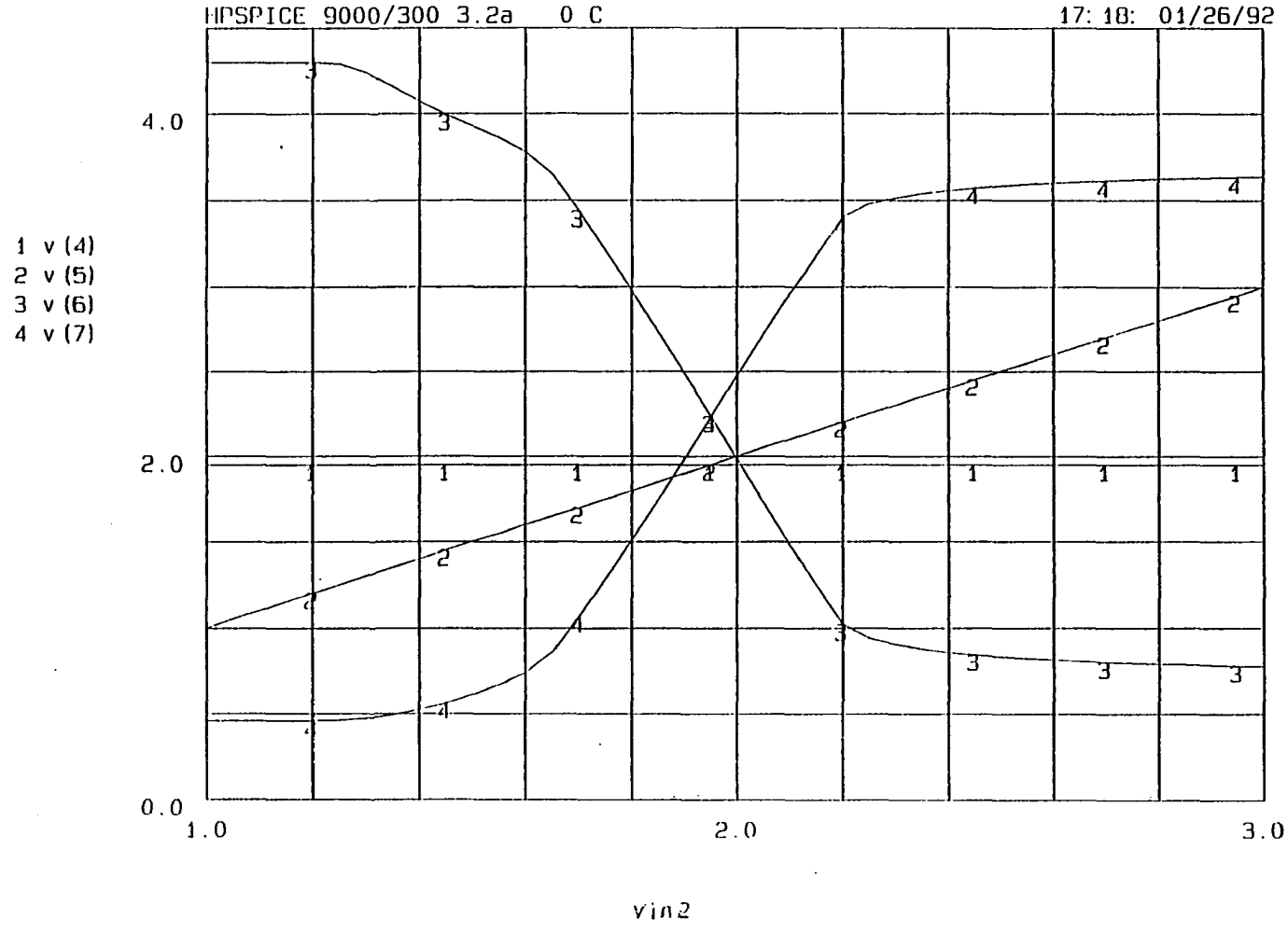

Figure A.2 Preamplifier Transfer Characteristics at 0°C

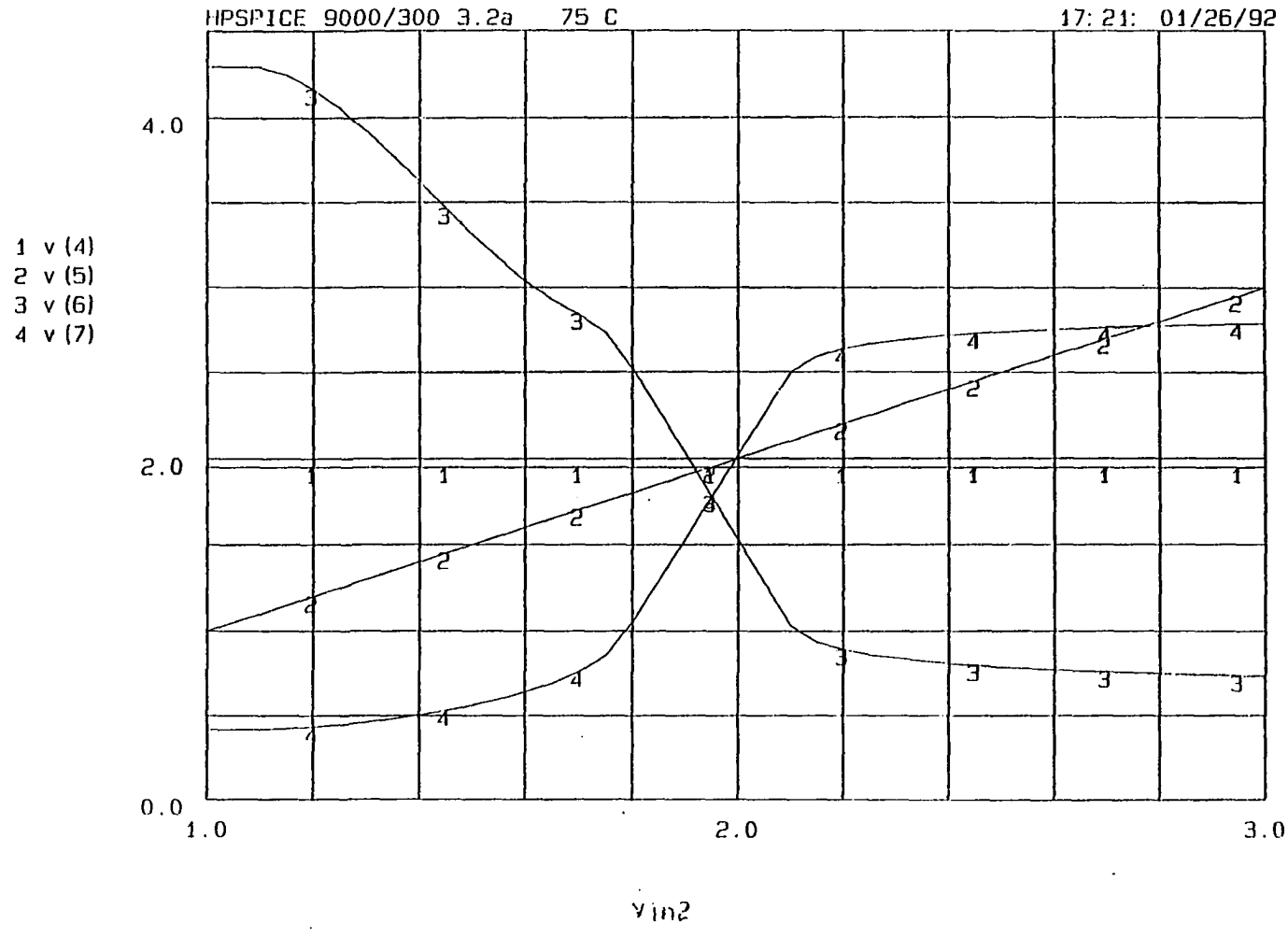

Figure A.3 Preamplifier Transfer Characteristics at 75°C

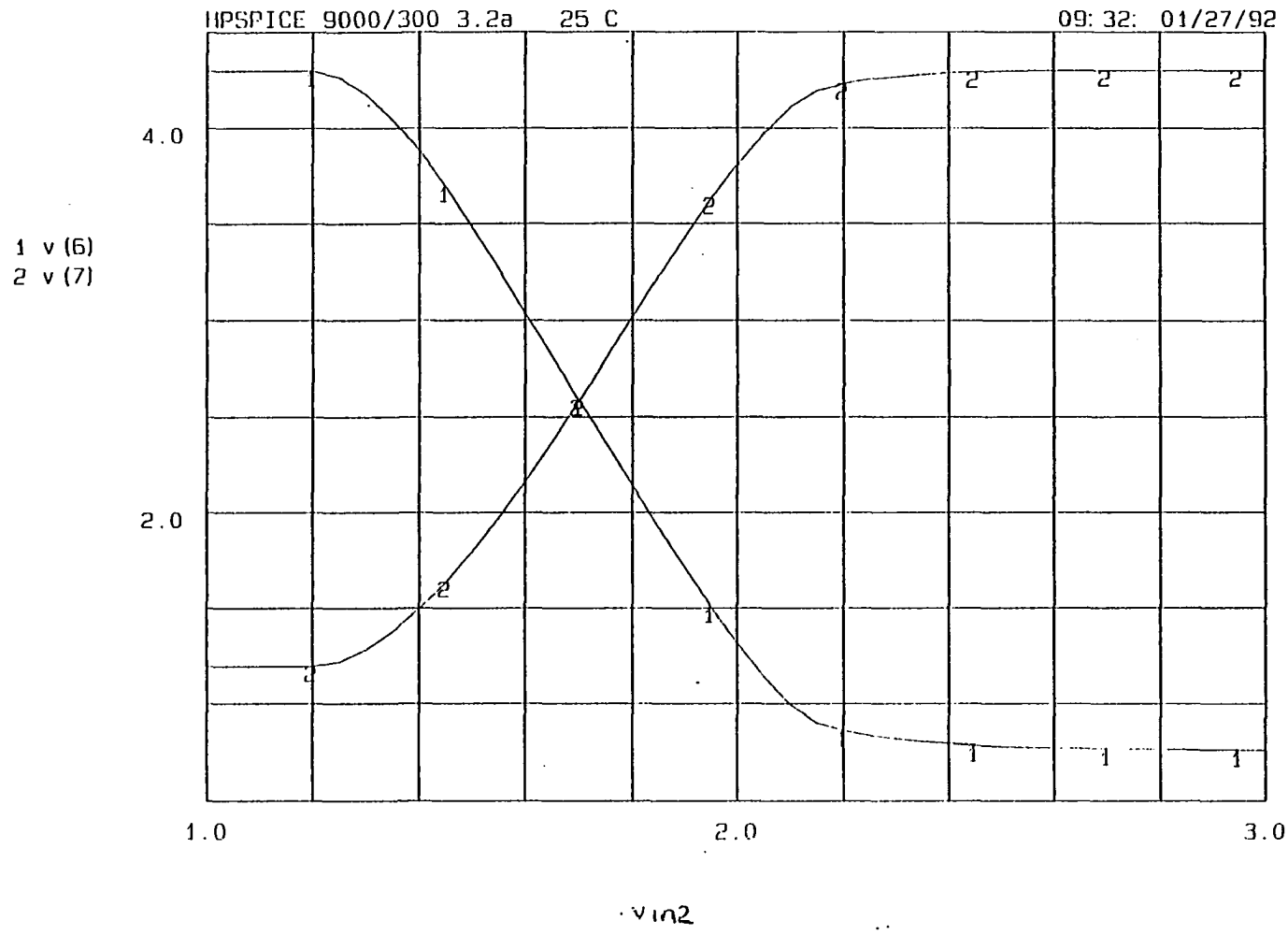

Figure A.4 Preamplifier Transfer Characteristics with 1.7V common mode signal and Vt=1.0V

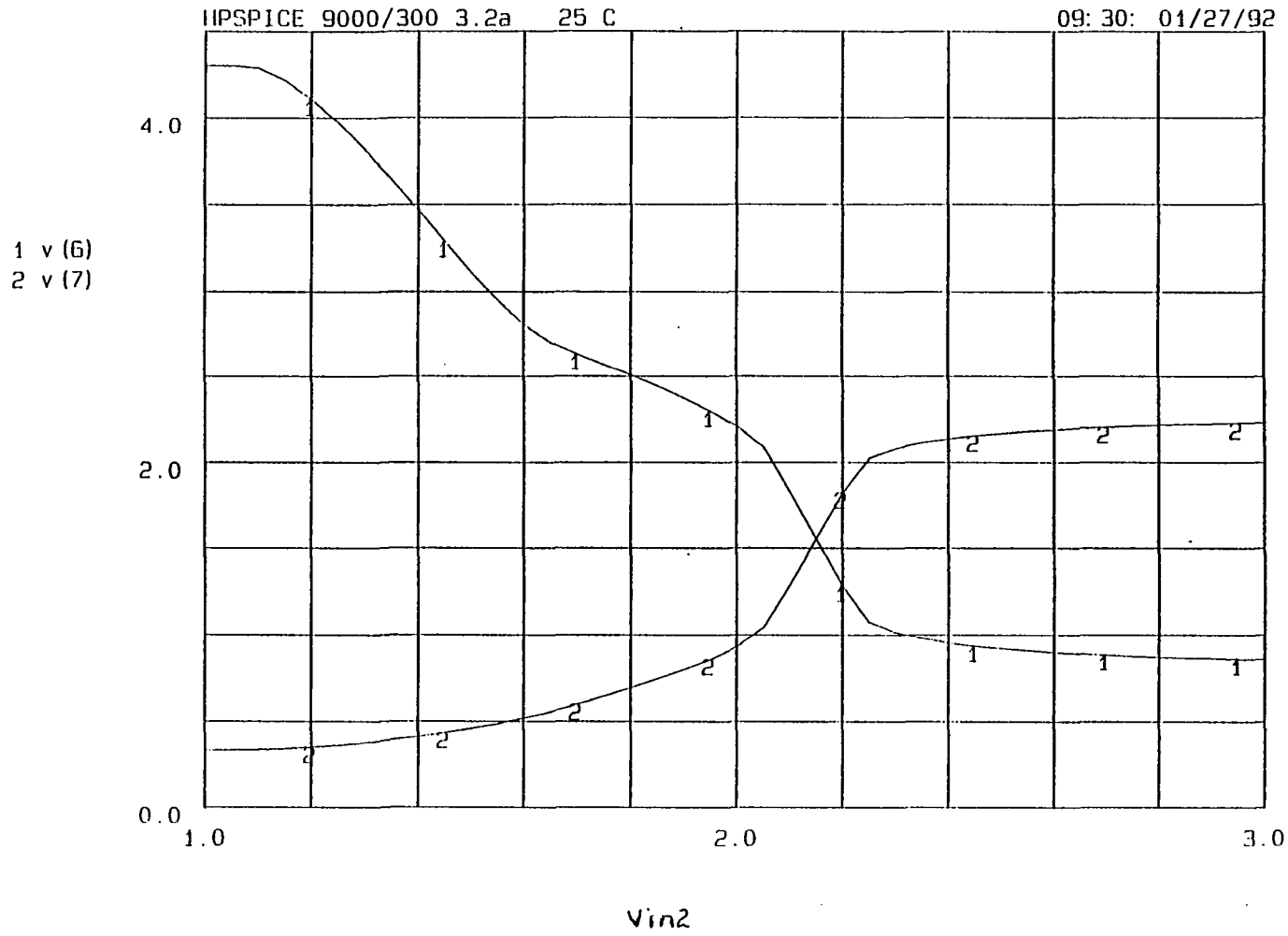

Figure A.5 Preamplifier Transfer Characteristics with 2.15V common mode signal and Vt=0.9V

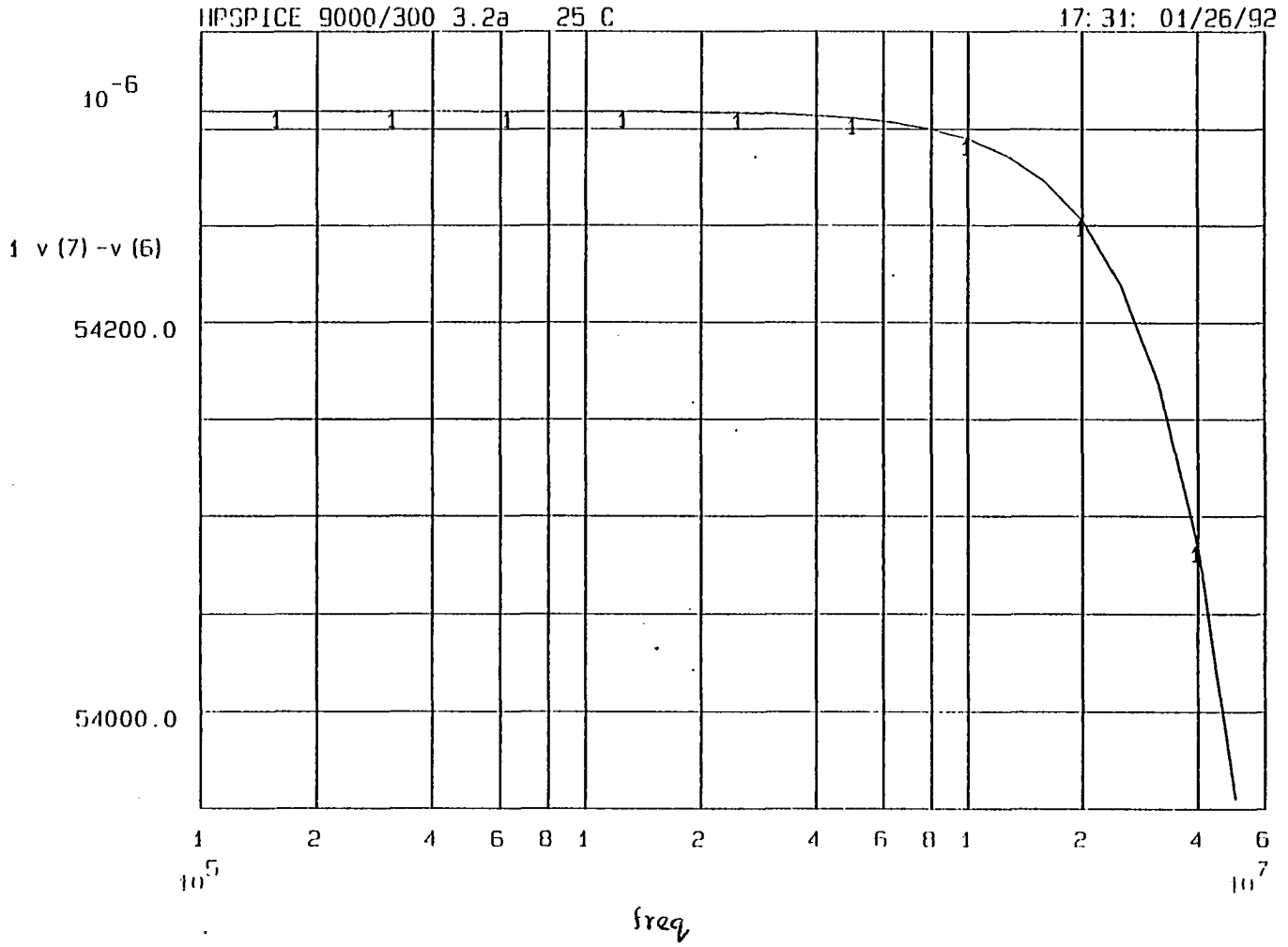

Figure A.6 Frequency Response of the Preamplifier

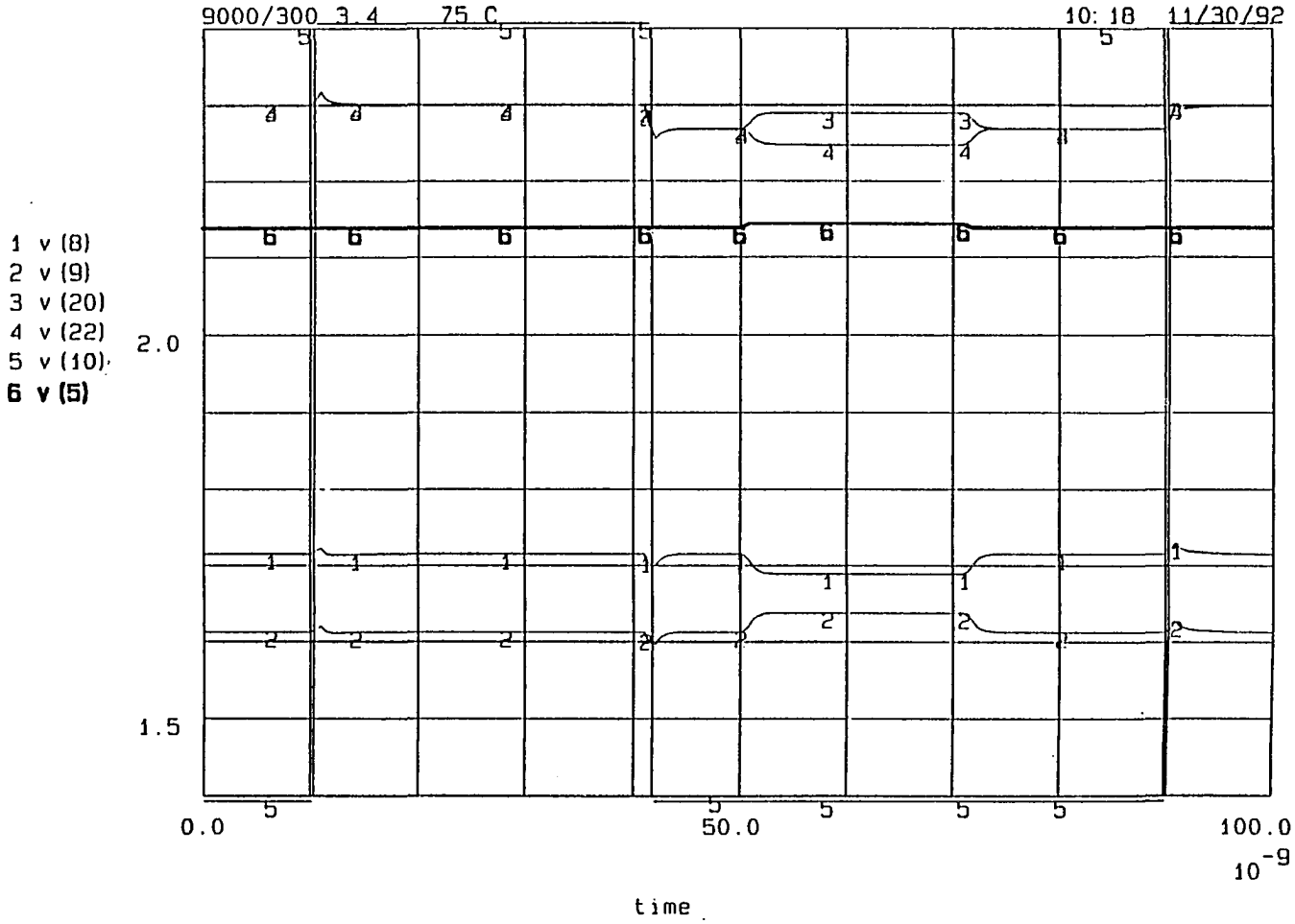

Figure A.7 Transient Response of the Autozero Circuit